FINITE STATE MACHINES
II. General FSMs
The State of the Machine

• The state can be encoded with a compact binary representation
  – Ex: 5 states
  – Minimum number of state bits = \( \text{ceil}(\log_2(5)) = 3 \) bits
  – Total possible states with 3 bits = \( 2^3 = 8 \)
  – There is probably limited value in optimizing which 5 of the 8 possible states you choose despite the fact you may have spent time looking at this in EEC 180A / EEC 18. You could try in a critical situation.
II. General FSMs
The State of the Machine

- The state can be encoded with a “one-hot” representation
  - Ex: 5 states
    - Number of state bits = Number of states = 5 bits
  - No min, no max, no optimizing
  - 00001
  - 00010
  - 00100
  - 01000
  - 10000
  + Zero-time state decode logic
  + Very fast state increment (shift not addition)
  - Not practical for a very large number of states
II. General FSMs
The I/O of the Machine

• Typically the **outputs** of FSMs are derived from the state but often not a copy of the state as is often true with counters

• Mealy machines have outputs that are functions of the inputs which creates a purely-combinational path through the FSM from input to output which could limit the maximum clock frequency
II. General FSMs
Major Components

- FSMs contain two major circuit structures
  1) Next State combinational logic
  2) State register (row of FFs with their clocks tied together)
- We could also include a third—output logic which is a function of state (Moore) or state and inputs (Mealy)
- Both (1) and (2) are usually coded with `always` blocks in verilog
- Always keep a clear picture of the output(s) and input(s) of each
- The Next State logic in this example:
  - output(s)  `state_c`
  - input(s)  `state, reset, abc, xyz`
II. General FSMs

**Next State Logic**

- Give thought to the logic you are creating
- In many cases, it will be best to write statements that directly use inputs of the Next State logic rather than other internal combinational logic variables
- In the example below, the longest path from the input(s) to the output `state_c` passes through three adders and a case selector (mux)

```verbatim
//--- Next State combinational logic
always @(freq or xyz or abc or reset) begin
  // logic
  d = abc + 8'h01;  // no issues
  e = d + 8'h01;   // creates state + 2
  f = e + 8'h01;   // creates state + 3
  case (state)
    3'b000: state_c = d;
    3'b001: state_c = e;
    default: state_c = f;
  endcase
end
```

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II. General FSMs

Next State Logic

- In the example below, the longest path from the input(s) to the output state_c passes through one adder and a case selector (mux)
- Even though the critical path is far shorter than the critical path of the previous example, the function is exactly the same

```verbatim
//----- Next State combinational logic
always @(freq or xyz or abc or reset) begin
  // logic
d = abc + 8'h01;   // no issues
e = abc + 8'h02;   // creates state + 2
f = abc + 8'h03;   // creates state + 3

  case (state) begin
    3'b000: state_c = d;
    3'b001: state_c = e;
    default: state_c = f;
  endcase

end
```
II. General FSMs

Next State Logic

- Example Next State combinational circuit with output \( \text{freq}_c \)
  - Always declare default values at beginning of always blocks
  - Use all of the best combinational logic design practices

```verilog
//--- Next State combinational logic
always @(freq or xyz or abc or reset) begin
  // defaults
  freq_c = freq; // an example

  // logic
  case (freq)
    ...
  endcase

  // logic
  if (xyz==4'b0010) begin
    ...
  end

  // reset logic is usually last for highest priority
  if (reset == 1'b1) begin
    freq_c = 3'b000;
  end
end
```
Five Things in Virtually Every Well-Designed Verilog State Machine

1) Default: \texttt{state\_c = state;}
2) \texttt{case (state)}
3) \texttt{STATE: begin ............. end} for each state. Partition design by \texttt{state}.
   (In traditional 180A-style design, we partition the overall design by \texttt{bits of the state}.)
4) \texttt{if (reset == 1'b1)} at the end of the combinational \texttt{always} block
5) Instantiate FF register(s) in a separate \texttt{always} block

// Next State combinational logic
always @(state or reset or ...) begin
  // defaults
  state\_c = state; // hold previous state
  case (state) begin
    INIT: begin
      ...
    end
    // Add a case target for each state
    default: c\_freq = 3'bxxx; // error case
  endcase
  // reset logic often last for highest priority
  if (reset == 1'b1) begin
    state\_c = 3'b000;
  end
end

// instantiate the state register
always @(posedge clock) begin
  state <= #1 state\_c;
end
Characteristics of a Well-Designed Verilog State Machine with Integrated Counters

1) In the default section, it is probably a good idea to have an auto-increment or auto-decrement statement
   - `count_c = count + 8'h01;` // Example increment
   - `count_c = count - 8'h01;` // Example decrement

2) In the “idle” or “wait” state, it is probably a good idea to hold the counter value to eliminate unnecessary toggling to reduce power dissipation
   - `count_c = count;` // Example hold counter value
   - `count_c = 8'h00;` // Example hold counter at zero
Finite State Design Example

- There are four states
  - **IDLE**
    - Go to PREP when go is asserted
  - **PREP**
    - Do something for 10 cycles
    - Then go to JOB1 if \( x \leq 5 \)
    - Then go to JOB2 if \( x > 5 \)
  - **JOB1**
    - Do something for 5 cycles
    - Then go to IDLE
  - **JOB2**
    - Do something for 20 cycles
    - Then go to IDLE
- \( reset \) at any time returns controller to IDLE state
State Diagram

- State diagram

- State transition diagram:
  - IDLE
  - PREP
  - JOB1
  - JOB2

  - From IDLE, go to PREP after 10 cycles.
  - From PREP, if $x \leq 5$, go to IDLE after 5 cycles.
  - From PREP, if $x > 5$, go to JOB2 after 20 cycles.
  - From IDLE, reset to IDLE.
  - From JOB1, go to JOB2 after 5 cycles.
Control Block Example Solution
(There are many solutions!)

• What are the registers (the values that need to be remembered)?
  1. state for the main controlling state machine
  2. count to count number of cycles in some of the states

• State registers
  – Choose two bits (obviously the minimum) for the four states

• Counter(s)
  – Choose three counters, one for each use – wasteful
  – Choose one five bit counter since states are independent and counter can be shared between different states
  – Counting down may be slightly better (simpler shared comparator for all cases that compare with zero when done)

• Keep registers (flip-flops) separate from state machine logic
  – Always do this for this class

• It is normally clearer to define states with names (such as IDLE) rather than constants (such as 2'b01)
The Circuit diagram in this case is very similar to the detailed block diagram.

- **Inputs**: reset, go, x[7:0]
- **FFs**: state[1:0], count[4:0]
- **Outputs**: not specified, probably driven by state[1:0]
Example Verilog Implementation

fsm.v

parameter IDLE = 2'h0; // constants in hex notation
parameter PREP = 2'h1;
parameter JOB1 = 2'h2;
parameter JOB2 = 2'h3;

reg [1:0] state, c_state; // declare both FF regs
reg [4:0] count, c_count; // and comb. logic regs

// Combinational logic for state machine
always @(state or count or go or x or reset) begin
  // defaults (place first)
  c_state = state; // default same state
  c_count = count - 5'b00001; // default count down

  // main state machine logic
  case (state)
    IDLE: begin
      if (go == 1'b1) begin
        c_state = PREP;
        c_count = 5'd09; // constant in decimal
      end
      else begin
        c_count = 5'd00; // only for lower power
      end
    end
    PREP: begin
      if (count == 5'b00000) begin
        if (x <= 8'd005) begin // assume 8-bit x
          c_state = JOB1; // goto JOB1
          c_count = 5'd04;
        end
        else begin // goto JOB2
          c_state = JOB2;
          c_count = 5'd19;
        end
      end
    end
    default: begin // good practice, but not used here
      c_state = 2'bxx; // better for testing
      c_state = IDLE; // another option
    end
case
  // reset logic (place last to override other logic)
in (reset == 1'b1) begin
  c_state = IDLE;
  c_count = 5'b00000;
end

end // end of always block

// Instantiates registers (flip-flops)
always @(posedge clk) begin
  state <= #1 c_state;
  count <= #1 c_count;
end

I think it is better to put reset logic inside the control logic rather than with the FF declaration.
NCVerilog simulation

- `reset_cold` to reset the clock oscillator
- `reset` to reset the state machine
- IDLE $\rightarrow$ PREP $\rightarrow$ JOB1 (since $x[7:0] \leq 8^{'d}05$)
Design Compiler Synthesis
Complete Gate Netlist

DFF_X1 \count_reg[2] ( .D(c_count[2]), .CK(clk), .Q(count[2]), .QN(n35) );
DFF_X1 \count_reg[3] ( .D(c_count[3]), .CK(clk), .Q(count[3]) );
DFF_X1 \count_reg[4] ( .D(c_count[4]), .CK(clk), .Q(count[4]) );
DFF_X1 \count_reg[1] ( .D(c_count[1]), .CK(clk), .Q(count[1]) );
DFF_X1 \count_reg[0] ( .D(c_count[0]), .CK(clk), .Q(count[0]), .QN(N8) );
XOR2_X1 U33 ( .A(count[3]), .B(n33), .Z(n29) );
XNOR2_X1 U34 ( .A(count[4]), .B(n34), .ZN(n30) );
OAI22_X1 U36 ( .A1(n21), .A2(n42), .B1(n40), .B2(n18), .ZN(c_count[2]) );
NOR3_X1 U41 ( .A1(count[1]), .A2(count[0]), .A3(n26), .ZN(n17) );
OR3_X1 U42 ( .A1(count[4]), .A2(count[3]), .A3(count[2]), .ZN(n26) );
OAI22_X1 U45 ( .A1(reset), .A2(n20), .B1(n21), .B2(n30), .ZN(c_count[4]) );
OAI22_X1 U46 ( .A1(reset), .A2(n22), .B1(n21), .B2(n29), .ZN(c_count[3]) );
OAI22_X1 U47 ( .A1(reset), .A2(n20), .B1(n21), .B2(n31), .ZN(c_count[1]) );
NOR2_X1 U53 ( .A1(reset), .A2(n25), .ZN(c_count[0]) );
NOR2_X1 U56 ( .A1(count[1]), .A2(count[0]), .ZN(n32) );
OAI21_X1 U57 ( .B1(count[0]), .B2(count[1]), .A(n32), .ZN(n31) );
NOR2_X1 U59 ( .A1(count[3]), .A2(n33), .ZN(n34) );
NAND3_X1 U27 ( .A1(n17), .A2(state[0]), .A3(N23), .ZN(n16) );
NOR2_X1 U43 ( .A1(n7), .A2(state[1]), .ZN(n23) );
INV_X1 U35 ( .A(n20), .ZN(n39) );
INV_X1 U37 ( .A(N10), .ZN(n42) );
INV_X1 U38 ( .A(N23), .ZN(n40) );
INV_X1 U39 ( .A(n23), .ZN(n43) );
INV_X1 U40 ( .A(n36), .ZN(n37) );
INV_X1 U44 ( .B1(n17), .B2(n43), .A(n4), .ZN(n24) );
INV_X1 U52 ( .A(reset), .ZN(n41) );
OAI21_X1 U54 ( .C1(N8), .C2(n24), .A(n39), .B(n38), .ZN(n25) );
INV_X1 U55 ( .A(n22), .ZN(n38) );
INV_X1 U61 ( .C1(x[2]), .C2(x[1]), .A(x[4]), .B(x[3]), .ZN(n36) );
NAND4_X1 U50 ( .A1(n16), .A2(n14), .A3(n41), .A4(n4), .ZN(n15) );
OAI21_X1 U51 ( .B1(n4), .B2(n14), .A(n18), .ZN(n28) );
OAI21_X1 U49 ( .B1(n7), .B2(n14), .A(n15), .ZN(n27) );
NAND4_X1 U50 ( .A1(n16), .A2(n14), .A3(n41), .A4(n4), .ZN(n15) );
OAI21_X1 U51 ( .B1(n4), .B2(n14), .A(n18), .ZN(n28) );
OAI21_X1 U49 ( .B1(n7), .B2(n14), .A(n15), .ZN(n27) );
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