Robust Clock Design

- Edge-triggered memory elements (flip-flops) are generally more robust than level-sensitive memory elements (transparent latches)
- Always follow these rules in this class, and for the most robust designs:
  1. Only clock signals may connect to flip-flop or latch clock inputs
     - A simpler circuit may sometimes be possible if a logic signal is connected to a clock input, but do not do it for robustness
     - always @(posedge key) begin
  2. Clock signals may not connect to any node other than a flip-flop or latch clock input
     - No logic gate inputs
     - No flip-flop or latch inputs other than the clock input
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- There are a few common exceptions to these rules—but they are topics outside the scope of this class. For example:
  - Clock generation circuits
  - Clock gating circuits
  - Clock tree buffer circuits

- These are circuit-level issues that must be designed carefully using *spice*