A more general method to drive a VGA monitor using the DE1-SoC

The DE1-SoC board has a 15-pin D-SUB connector designed for VGA (Video Graphics Array) video output. The VGA_controller.v module is designed so that the colors that are driven on the signals *ired*, *igreen*, and *iblue* will appear at the pixel location indicated by *col* and *row*. This document shows the block diagram, port names, and timing diagram of the provided VGA project.

The Top-Level Module Block Diagram

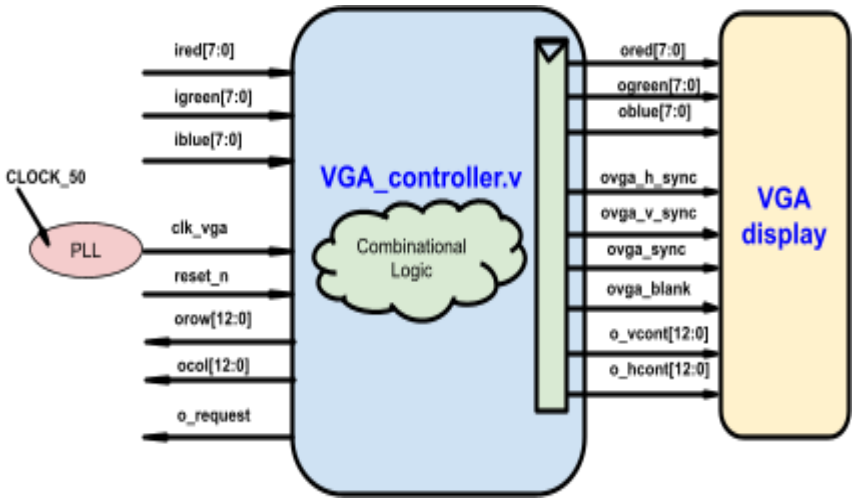

Figure 1. VGA_controller.v module and VGA display block diagram

Port names (Verilog)	Direction	Width	Description
clk_vga	Input	1	VGA clock @ 25.000 MHz
reset_n	Input	1	VGA reset, active low, asynchronous
ired	Input	8	The input value of red color
igreen	Input	8	The input value of green color
iblue	Input	8	The input value of blue color
ovga_sync	Output	1	VGA synchronization signal
ovga_ blank_n	Output	1	VGA blank signal, active low
ored	Output	8	The value of red color to VGA
ogreen	Output	8	The value of green color to VGA
oblue	Output	8	The value of blue color to VGA
ocol	Output	13	Indicates the horizontal pixel position (0 - 639)
orow	Output	13	Indicates the vertical pixel position (0 - 479)

o_hcont	Output	13	Vertical counter; Max (0 - 799); Valid (142 - 781)
o_vcont	Output	13	Horizontal counter; Max (0 - 524); Valid (36 - 515)
o_request	Output	1	o_request indicates the RGB input valid range

Table 1. Ports of VGA_controller.v

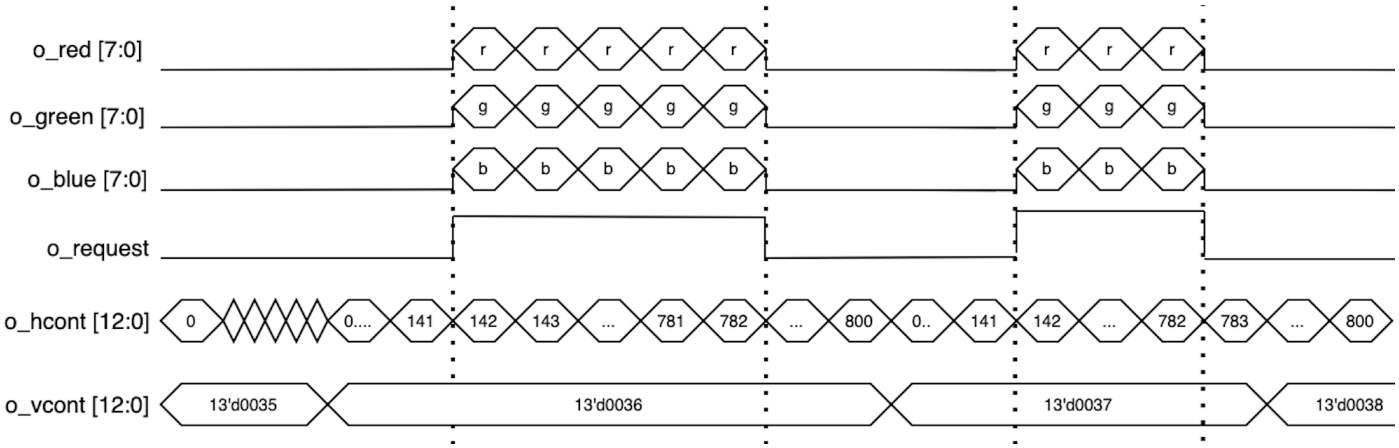

Figure 2. Key waveforms of VGA_controller.v