Using the Terasic D8M-GPIO camera with the DE1-SoC

The DE1-SOC and camera system captures images from the D8M-GPIO digital camera. The system converts the raw data from the camera to RGB format. This document shows the block diagram, port names, and timing diagram of the provided camera project.

The Top-Level Module Block Diagram

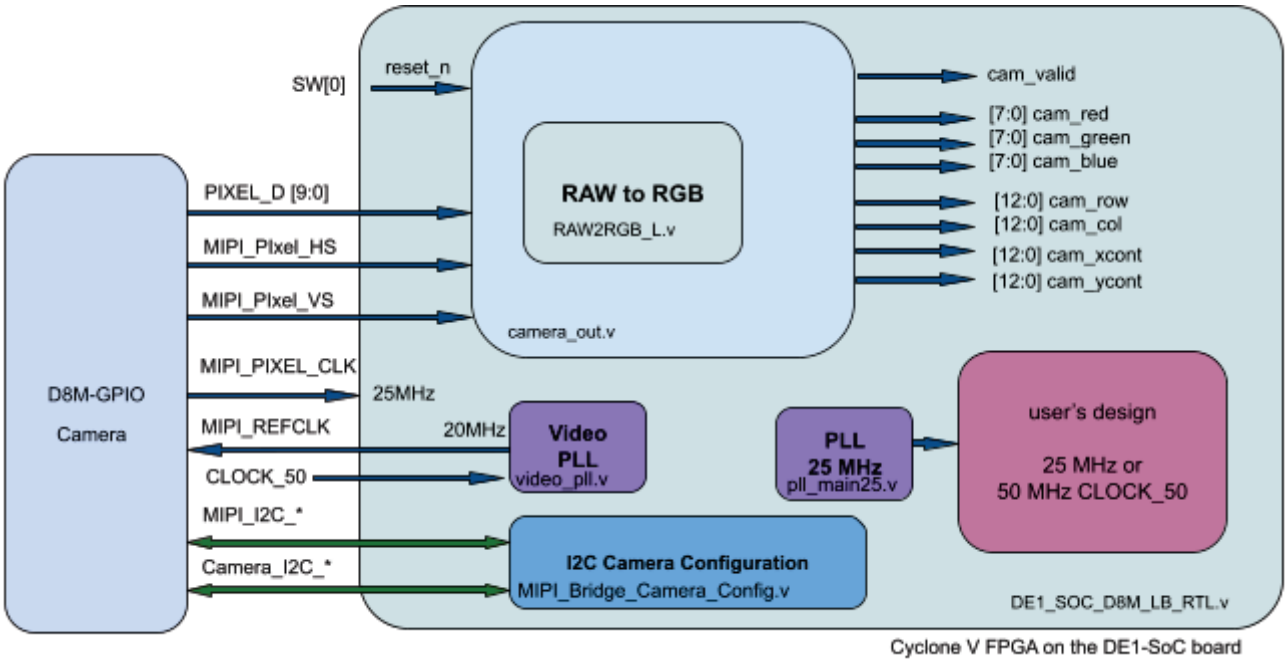

Figure 1. Top-level block diagram

Port Name (Verilog)	Direction	Width	Description
Clock_50	Input	1	Clock @50 MHz
PIXEL_D	Input	10	Camera input RAW data
cam_red cam_green cam_blue	Output Output Output	8 8 8	Pixel data in the RGB format
cam_col cam_row	Output Output	13 13	The col range of camera output (0 - 616) The row range of camera output (0 - 477)
cam_xcont cam_ycont	Output Output	13 13	Vertical counter (0 - 799) Horizontal counter (0 - 524)
cam_valid	Output	1	The pixel output data is valid

Table 1. Ports of verilog module camera_out.v

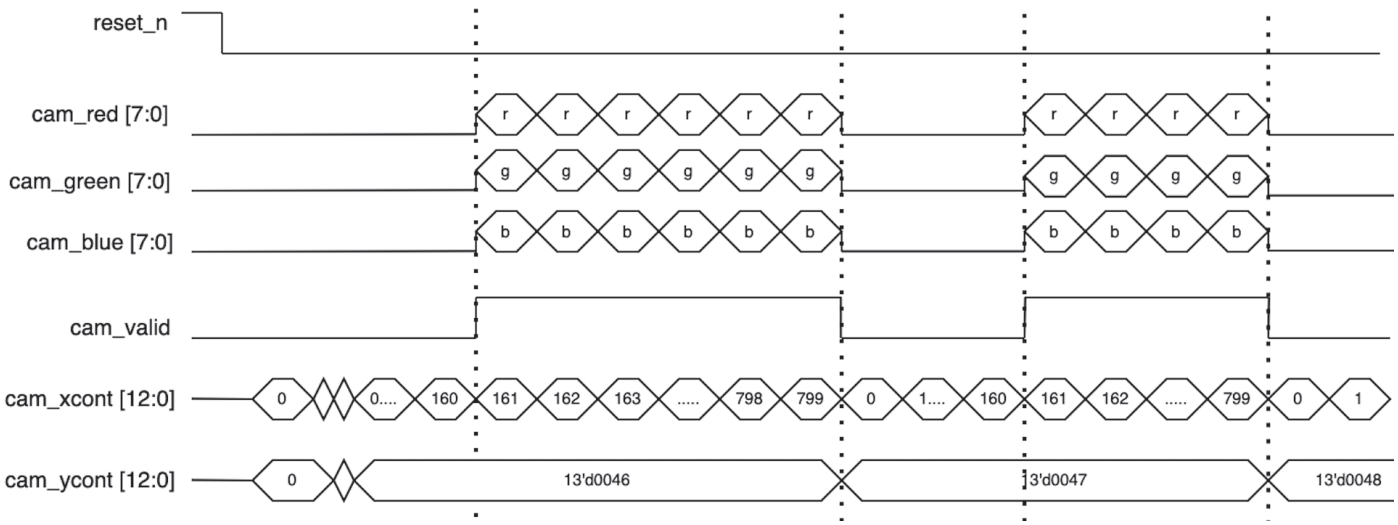

Figure 2: Waveform of the camera_out.v