Jan. 18

In testbench but not fsm

- H delay (except in FFs)
- Signed regs under test ok
- for loop
- if write
- if display

Test Bench 41

\[\text{Diagram of circuit} \]

\[\text{Waveform diagram} \]

\[\text{Input: } \text{in} = 0000, x = 0001, x = 1010 \]
Testbench #2

Four things in test verilog:

1. wire x;
   assign x = - - i;

2. reg y;
   always @ (inputs of y) begin
     y = - - i;
   end
3. `reg z;
   always @(pos edge clk) begin
       z <= #1 z & ~z;
   end

4. Instantiate a module