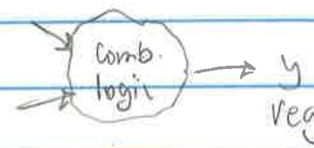
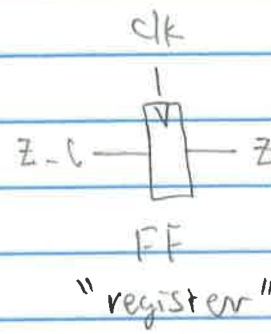
The only things in your HW verilog

①
```
wire x;
assign x = ~~~ ;
```

②
```
reg y;
always @ (inputs of y) begin
    y = ~~~ ;
end
```



③
```
reg z;
always @ (posedge clk)
    z <= #1 z_c;
end
```



④ instantiate a module