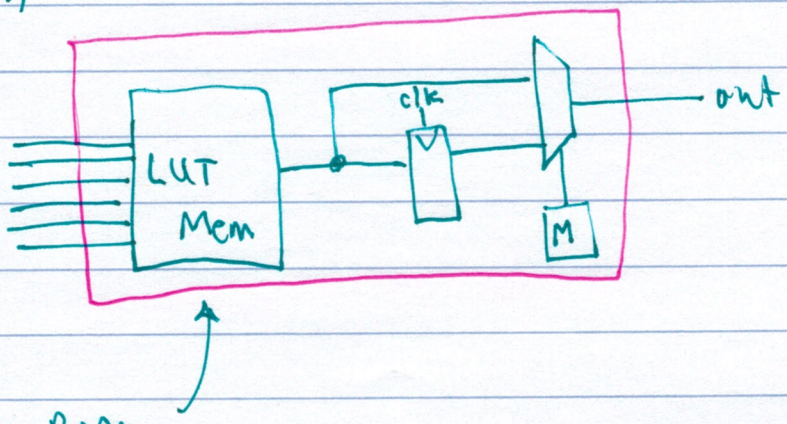
EEC 180 — LAST LECTURE!

June 3, 2021

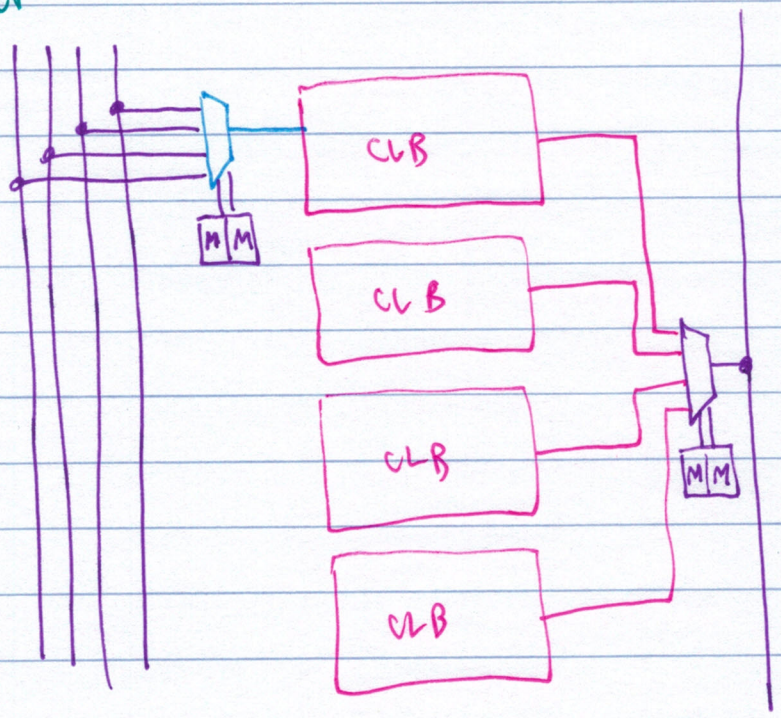
FPGAs

- Logic cells
  Comb. logic Blocks (CLBs)

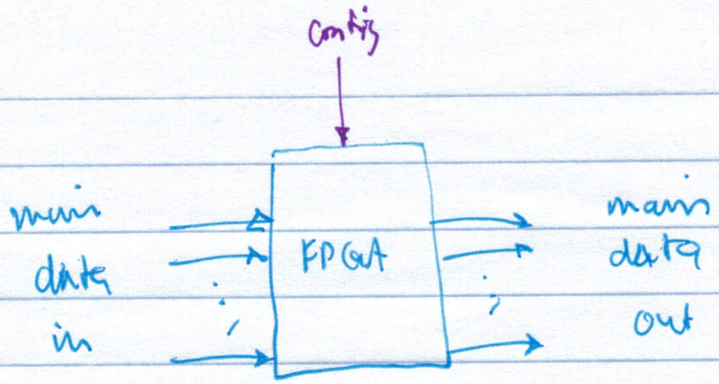


ROM
in normal function
(actually an SRAM)

- Interconnect

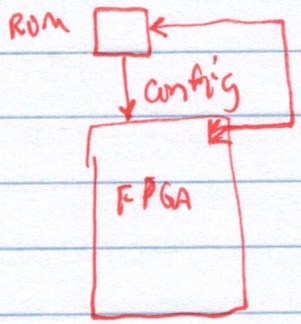


- User mode
- Programming mode



- JTAG interface controlled by a PC
- micro controller on board
- ROM on board

JTAG
- slow serial simple interface
- originally designed for an external tester to test a chip



1) Altera / Intel

- Stratix — High perf.
- Arria — Balanced cost, power perf.
- Cyclone — Low cost
- Max — " ", Non-volatile memory
  - * DE10-Lite
    Max 10

2) Xilinx

• Virtex	High end	364 K – 1,221 K LUTs
• Kintex	Balanced	41K – 298K LUTs
• Artix	Low power	8K – 134K LUTs
• Spartan	Low cost	3752 – 64,000 LUTs

LUT – Lookup table (ROM / SRAM)

6-inputs (64 words)

(2) 5-input tables (2 × 32 words)

"Slice"

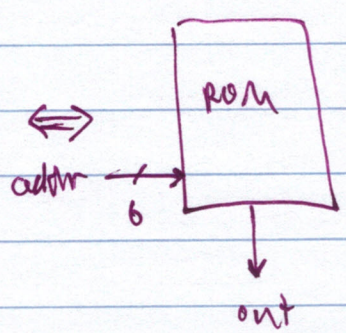
- 4 LUTs
- 4 FFs ⟷ latches
- muxes
- carry logic

Using LUTs

T.T.

A B C D E F	out
0 0 0 0 0 0	0/1
0 0 0 0 0 1	0/1
.	.
.	.
.	.
.	.
1 1 1 1 1 1	1

6-input AND

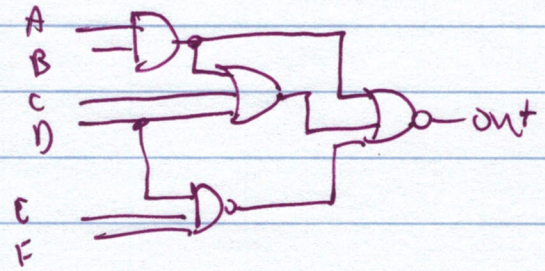


a) 6-input AND

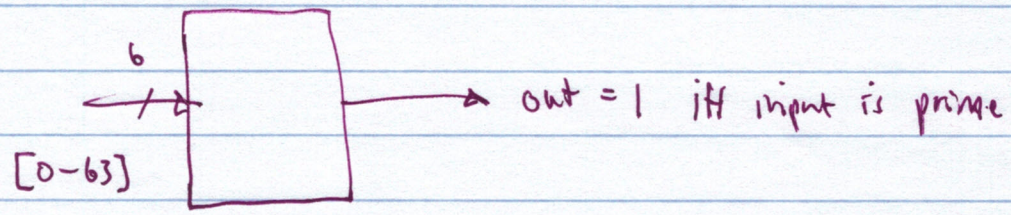
b) 2-input AND

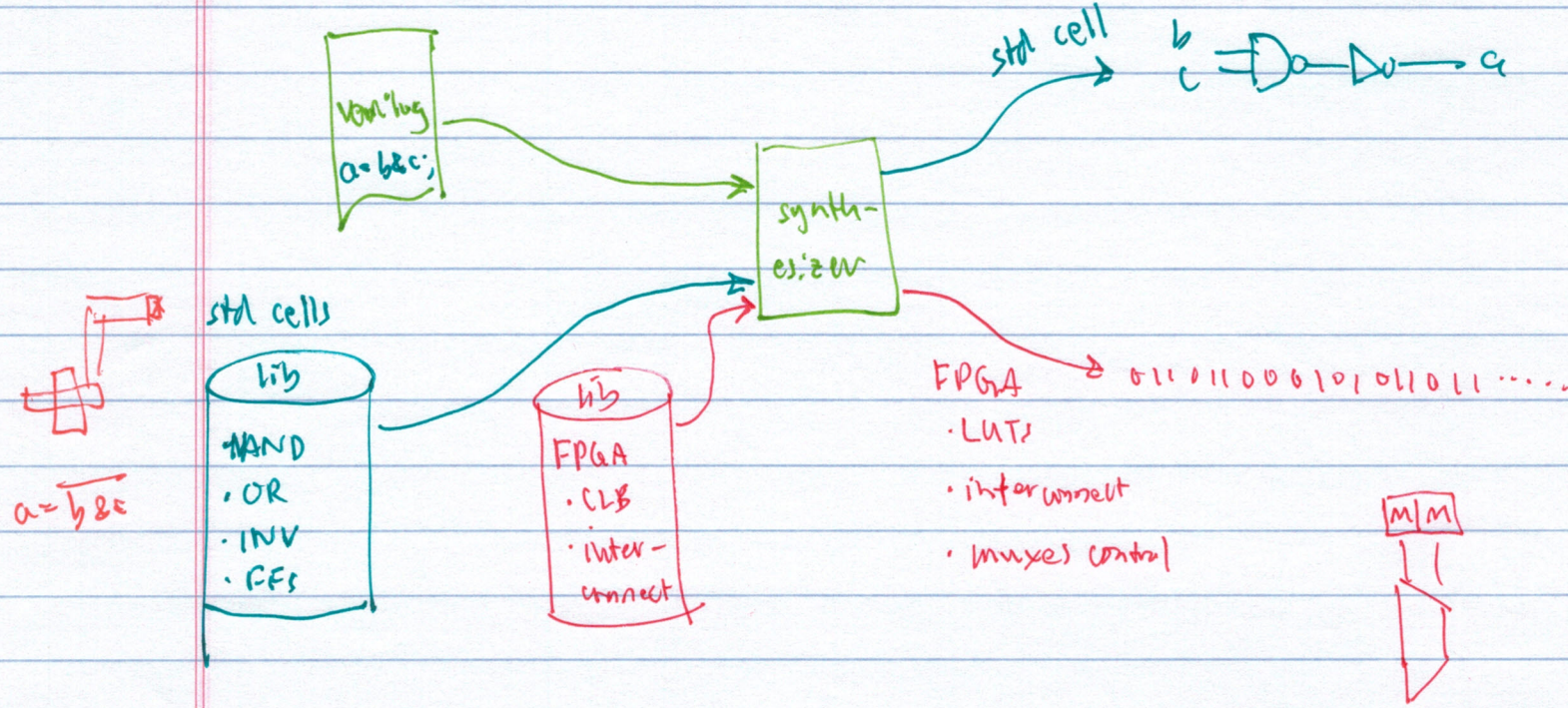
A	B	C	D	E	F	out
0	0	0				0
0	0	1				0
0	1	0				0
0	1	1				1
1	0	0				0
						0
						0
						1

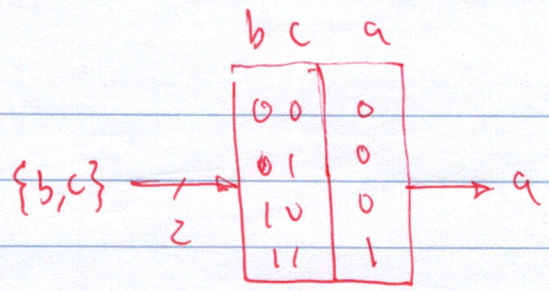
c)



d)



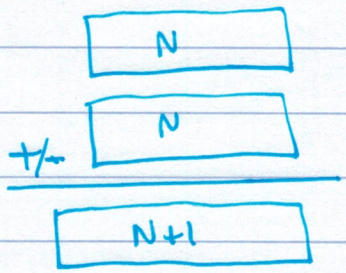




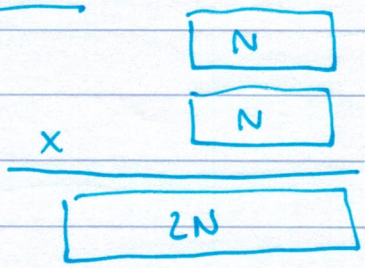
Word size and growth

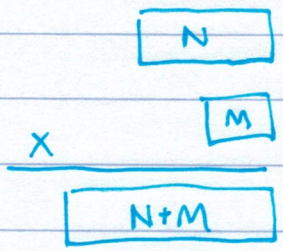
Must maintain accuracy → keep bits
Store, transmit data → reduce bits

Add / Sub

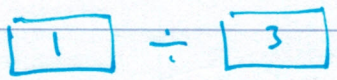


Mult



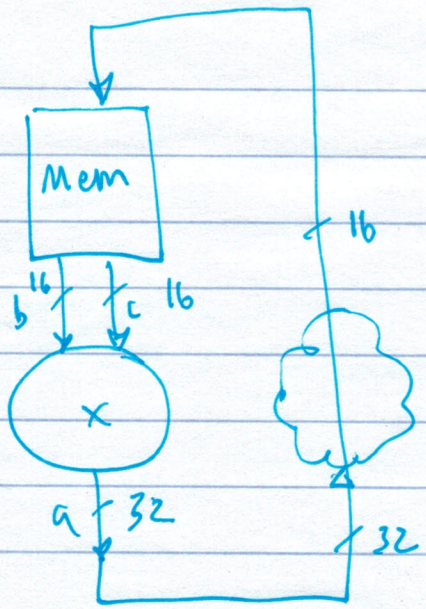


Divide



- No min width precision for quotient

$a = b \times c$



1) Rounding

0.XXXXXX

↓

0.XXX

HW:

1) truncation

2) Add ½ LSB and truncate

-3.5 → -3

3) "optimal"

-3.5 → -4

2) Saturation

- reduce from MSB side

XXXXXX

↓

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