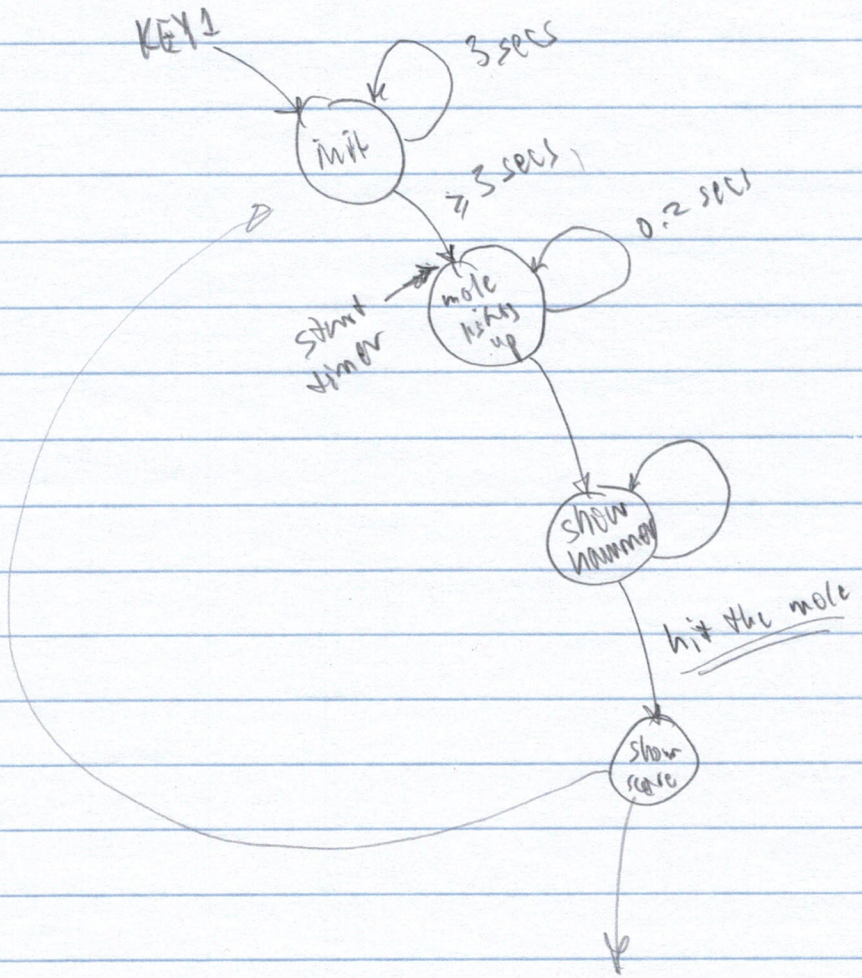
May 25, 2021

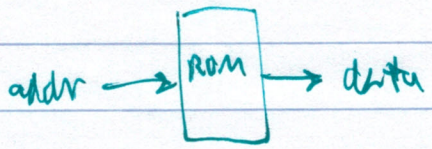


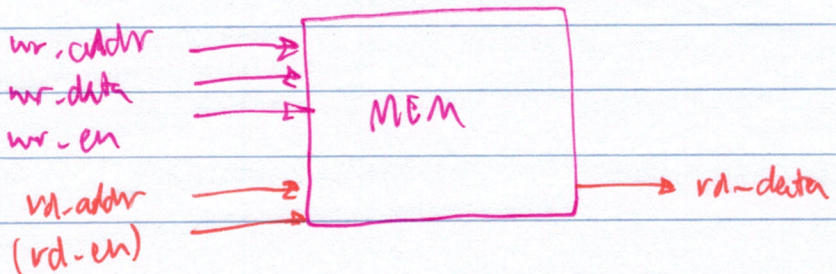
Memories

View 1
- Datapath
- Control
- Memory
  1) Single-bit
  2) Array

View 2
- Rd/Wr
  - SRAM
  - DRAM
- ROM
  - Basic ROM
  - PROM
  - synth. from std. cells
- Non-vol. RA/W
  - EPROM
  - Flash

View 3
- Combinational logic
  - ROM
- Feels comb.
  - PROM
  - EPROM
- Sequential
  - SRAM
  - DRAM
  - Flash



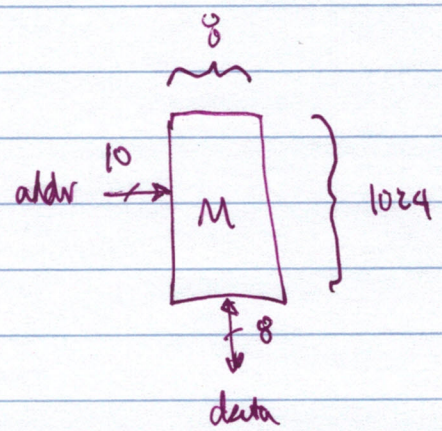


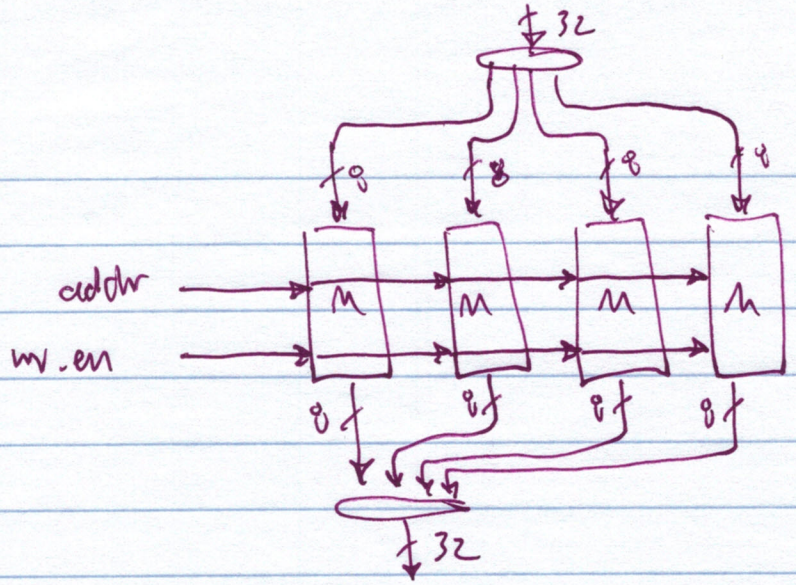
Bit-slicing

- Increase word width

- Ex: Have: 1K word x 8 bits (1024)
  Want: 1K word x 32 bits

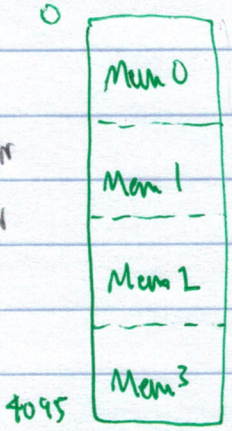
$\log_2(1024) = 10$

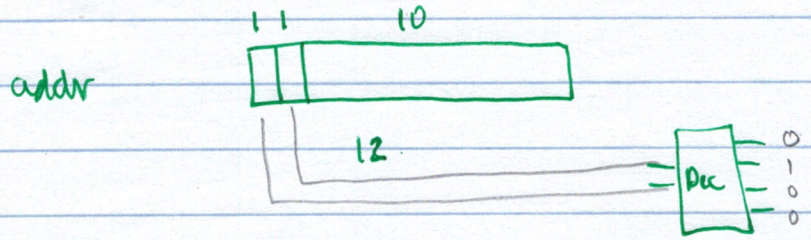


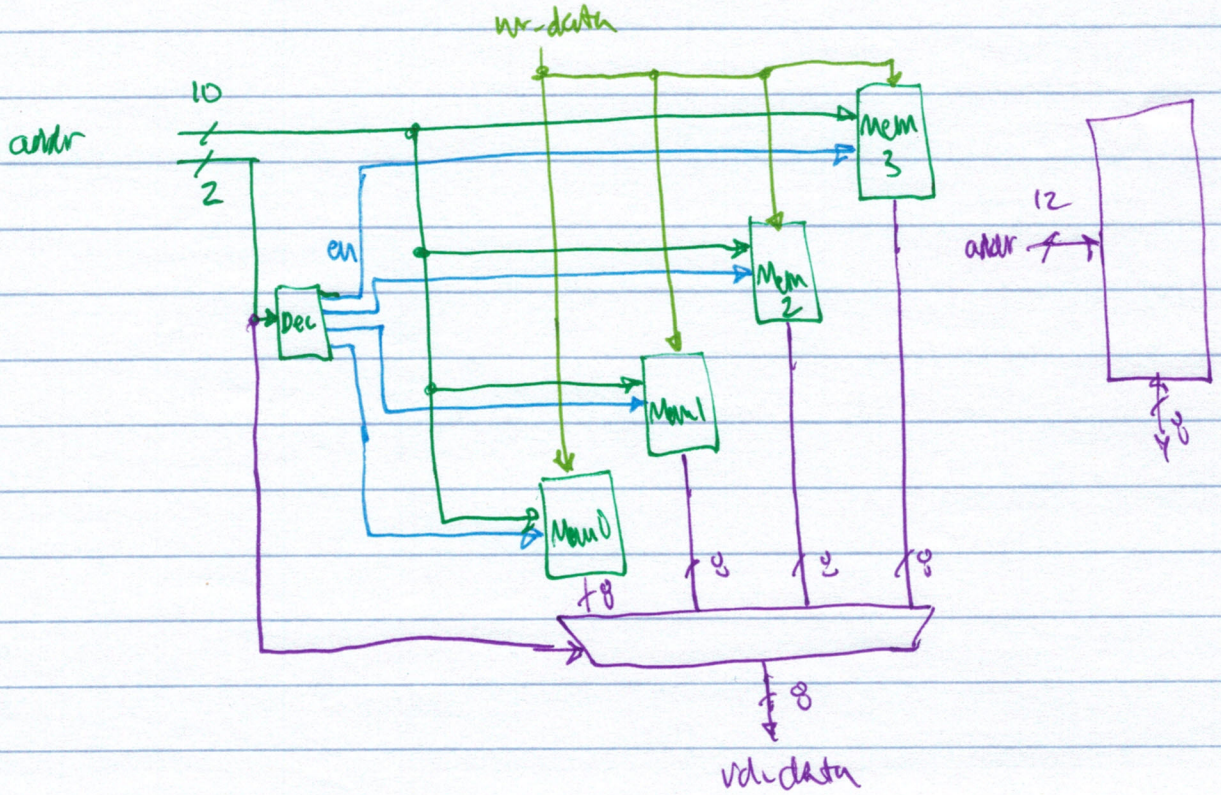


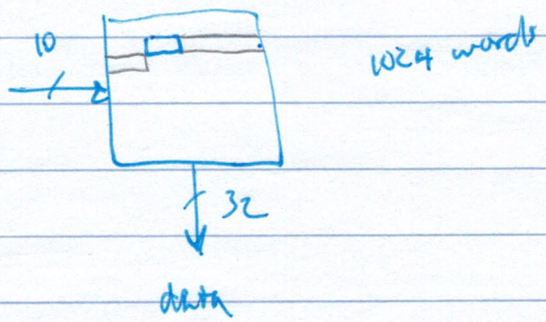
Banking

- Increase number of words
- Ex: Have: 1024 words x 8 bits 10-bit addr
  Want: 4KW x 8-bits 12-bit addr









Views 4

1) On-chip "macro"

2) Synth. from verilog
   A) Std. Cells
   B) FPGA CLBs

3) Off-chip
   - large DRAM
   - Flash

Verilog

Declare 16 bit x 128 word

```
reg [15:0] Mem [0:127];
```

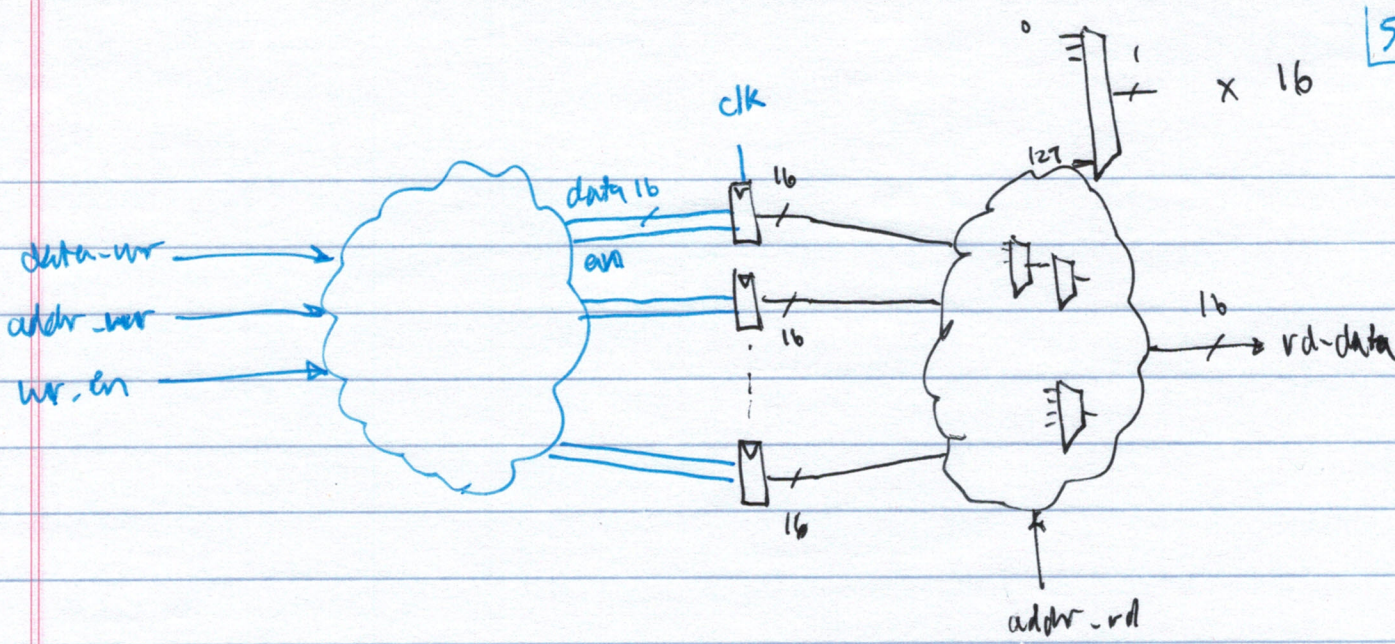
Read port (7-bit)

```
data_rd = Mem[addr_rd];
```

- combinational circuit
- think of it as a huge mux tree

Write

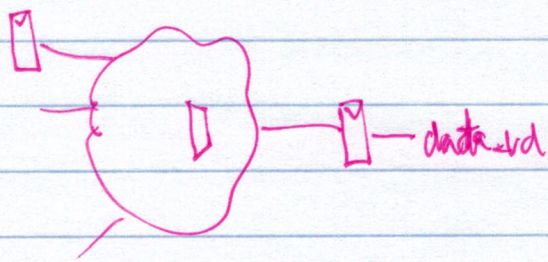
```
Mem[addr_wr] <= #1 data_wr;
```



"asynchronous" read

Synchronous Read

data_rd <= #1 Mem[addr_rd];



- this is how the M9K block RAM works

Total memory size = # words x # bits/word

$= 2^{addr} \times data\_width$