

Memories

May 20,
2021

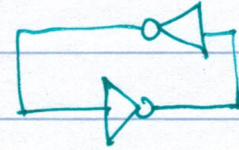
View 2

1) Read-Write Memories

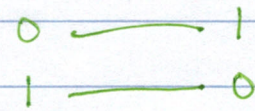
A) Static Random Access Mem. (SRAM)

cell - bistable element

back-to-back inverters



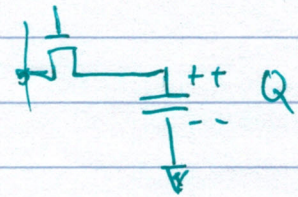
holds value until power is removed

 $\frac{1}{2}$ $\frac{1}{2}$ meta stable

B) Dynamic RAM - (DRAM)

- holds value for only a very short time $\sim < 1 \mu\text{sec}$

- requires refreshing



2) ROM - Read-Only memories

- Non-volatile

A) Basic ROM - values cast when chip is fabricated

B) Programmable ROM - PROM

- fuse

- anti-fuse

C) Synthesized from std cells - ASIC

CLBs - FPGA

3) Non-Volatile Rd/Wr Mem. - NVRWM

A) EPROM - Erasable Prog. ROM

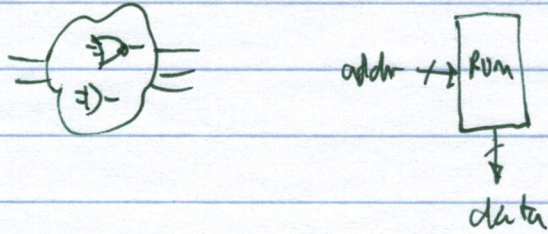
erasable w/ UV light

B) EEPROM - Elect. Eras. Prog. ROM - (Flash)

- erase electrically

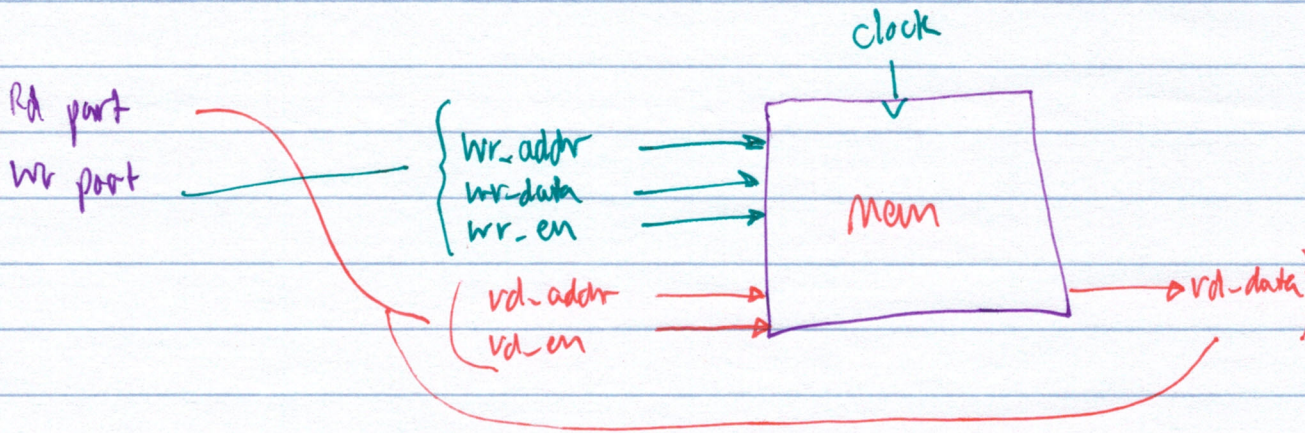
View 3

- 1) Combinational (output depends on only present inputs)
 - ROM



- 2) Feels Combinational but technically sequential
 - PROM
 - EPROM

- 3) Sequential (output depends on present + past inputs)
 - SRAM
 - DRAM
 - Flash



rd-en for power reduction

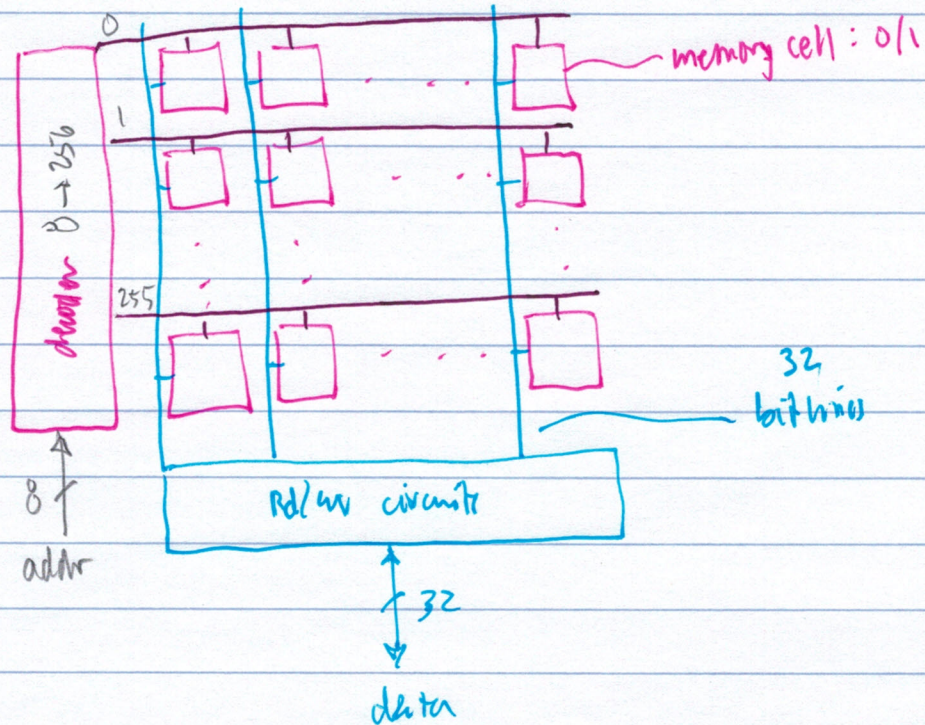
8 Kbit memory

256 word lines

3

Components

- array of cells
- addr decoder
- Wr circuitry
- Rd circuitry
- word lines
- bit lines



Interfaces

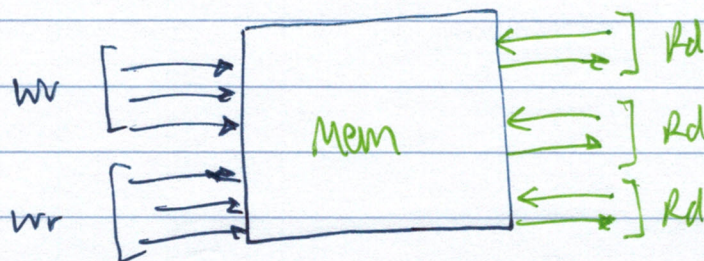
- Addr
- Data
- En-wr
- En-rd
- clock

Multi-ported SRAM

Ex: register file for classic RISC - 1 Wr + 2 Rds per cycle

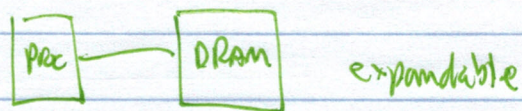
Ex: Itanium 22 ports (12 Rd + 10 Wr)

[USCC 2005]



DRAM

- Classic DRAM
- Embedded DRAM



View 4 - Memory types for custom chips

- 1) On-chip "macro" memory arrays
- 2) On-chip synthesized from verilog
- 3) off-chip

1) A) On-chip Macro Mem

Software tool to generate macro. We choose:

- # of words 256
- word width in bits 32
- # of rd ports
- # of wr ports
- rd/wr or R/W
- BIST - built-in self test

≡

Output:

- Verilog
- other CAD views

B) FPGA

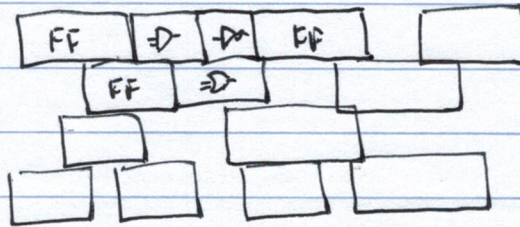
"Block RAMs"

- Altera M9K - 8K or 9K bits each
- 182 on chip

2) Verilog synths into std cells - =>

A) ASIC std cell =>

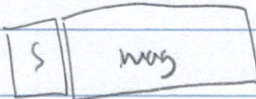
memory cells built w/ FFs =>



B) FPGA

Build w/ CLB elements

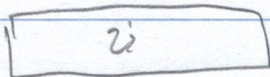
Our chip has 50,000



0 pos

0 zero

1 neg



-8 4 2 1