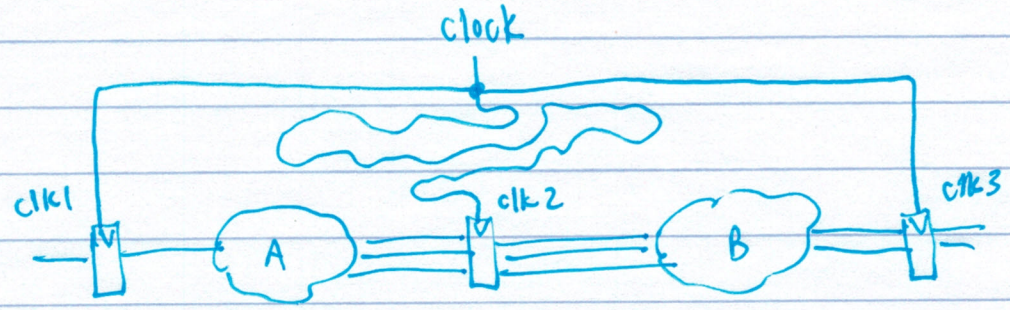
EEC 180

May 6, 2021

Requirement #2 - Logic is not too fast
Clock is not too skewed

An Aside

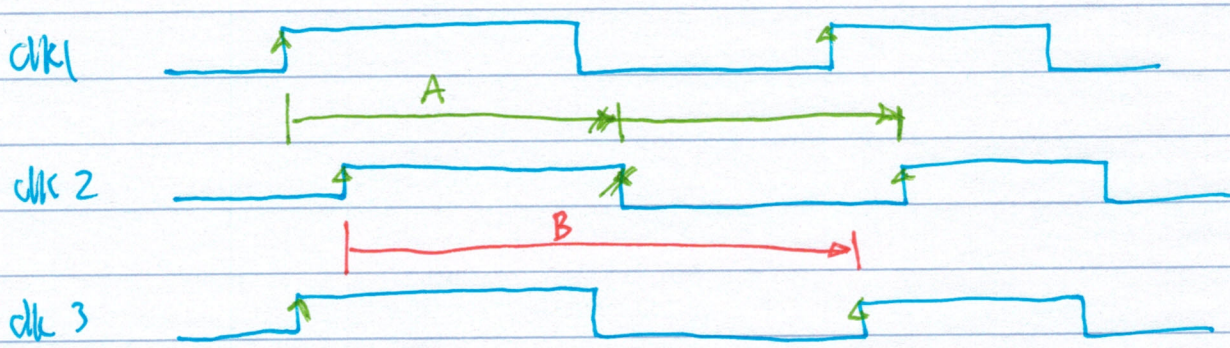


let $f_{clk} = 1.0\ GHz \rightarrow t_{cycle} = 1\ ns$

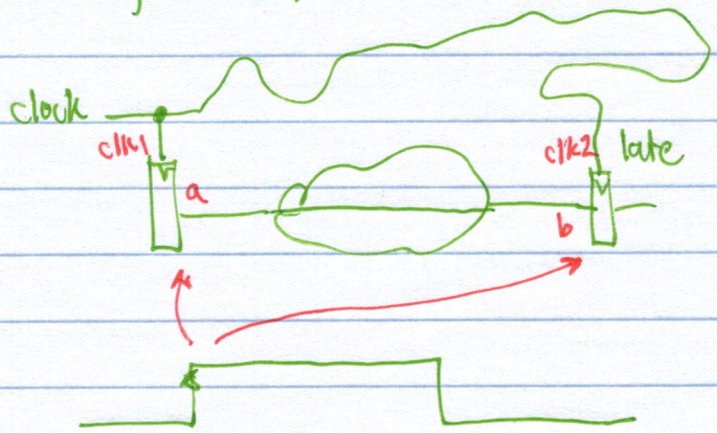
clk2 is 0.1 ns later than clk1 and clk3

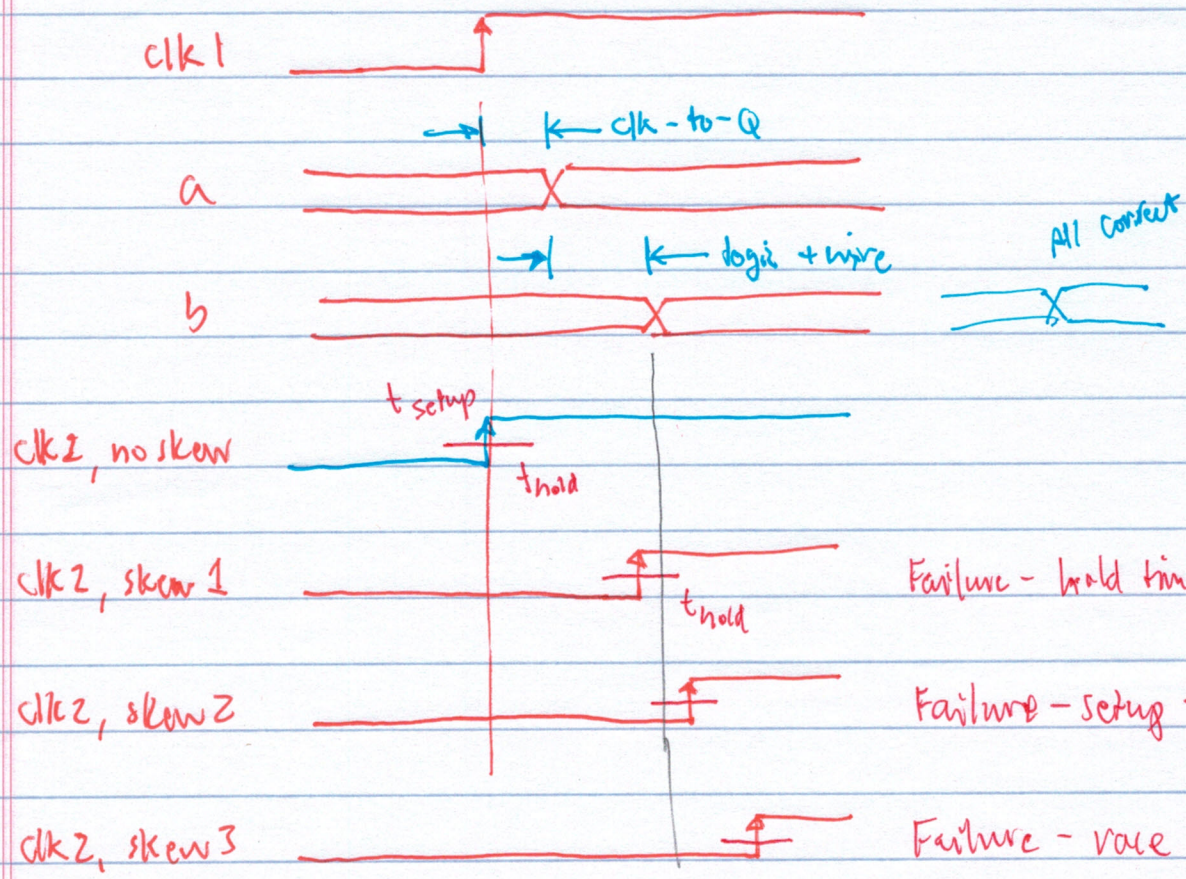
$t_{cycle_A} = 1.1\ ns$

$t_{cycle_B} = 0.9\ ns$

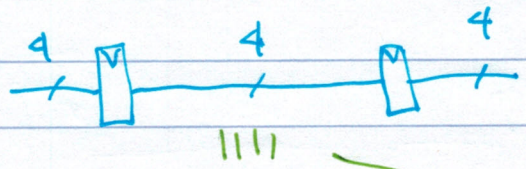


Enabled by clock skew



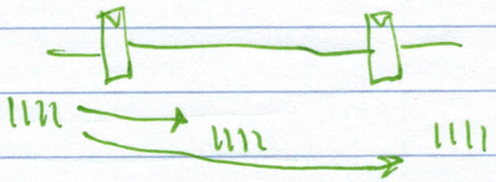


Timing violations



1111 correct
1011
1001
⋮

Worst case - race through clk skew



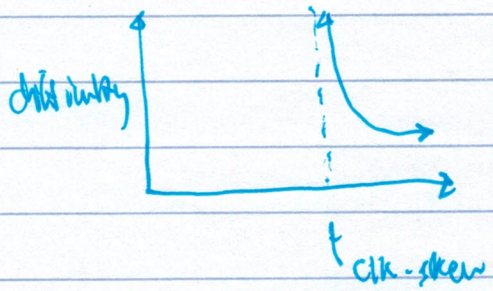
$$t_{clk\text{-}to\text{-}Q} + t_{logic_{min}} + t_{wire} > t_{clk\text{-}skew} + t_{hold}$$

for correct operation

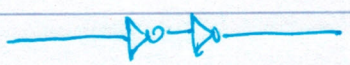
What if the requirement is violated?

At Design Time

- lower clock skew



- increase $t_{logic\ min}$



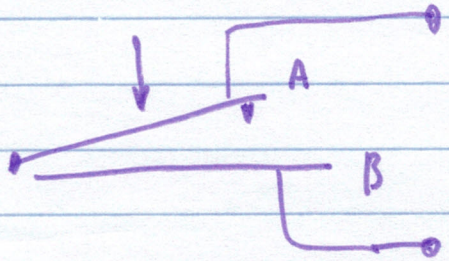
Very easy!
Add slow circuits

B) After chip is built
- all terms in eqn. are in silicon / chip
- no fixes possible!

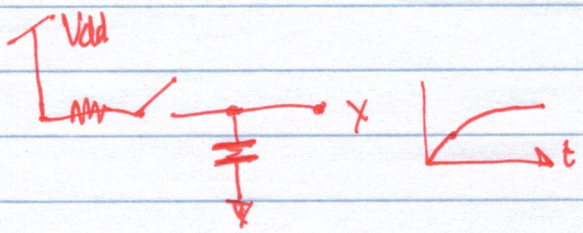
∴ Hold time violations are dangerous!

Interfacing with input signals

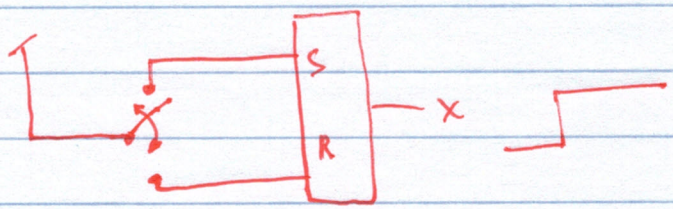
I. Debounce the input



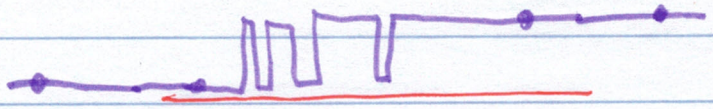
1) Low-pass filter, e.g. RC



2) Double-throw switch w/ an SR latch



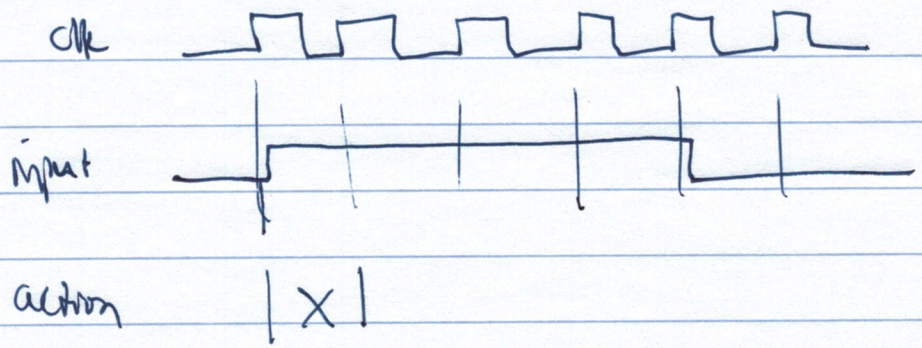
3) Some type of sampling or gating circuit



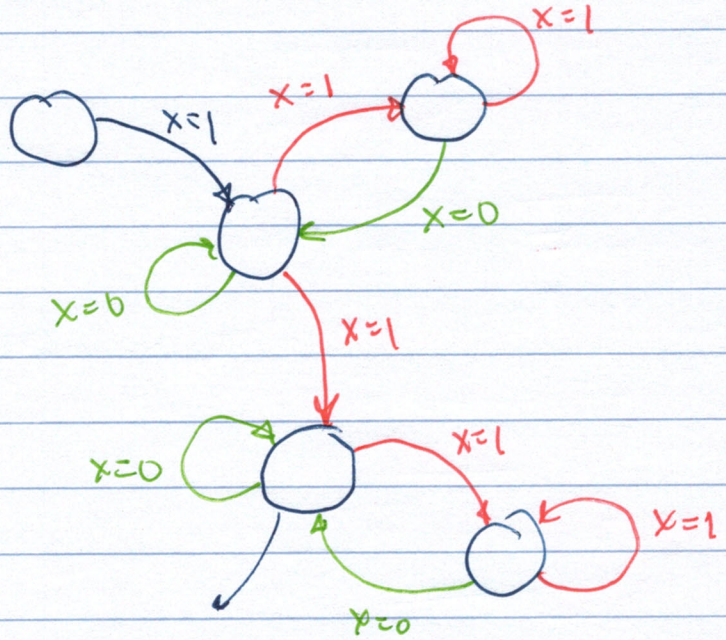
0 0 1 1

- DE-10 Lite debounces SW and KEY

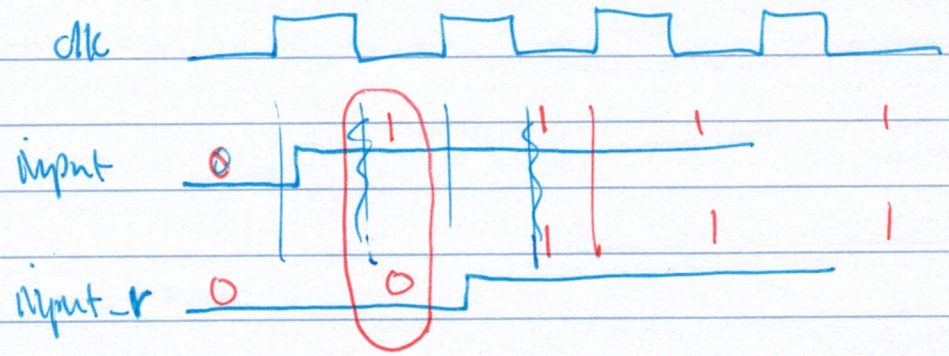
II. Edge Detection

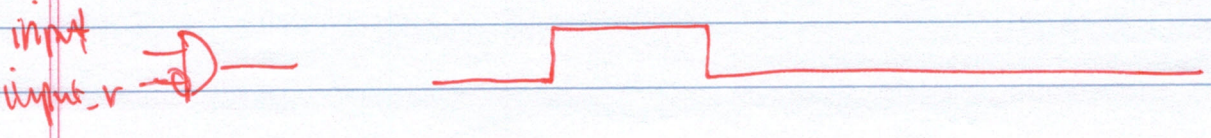


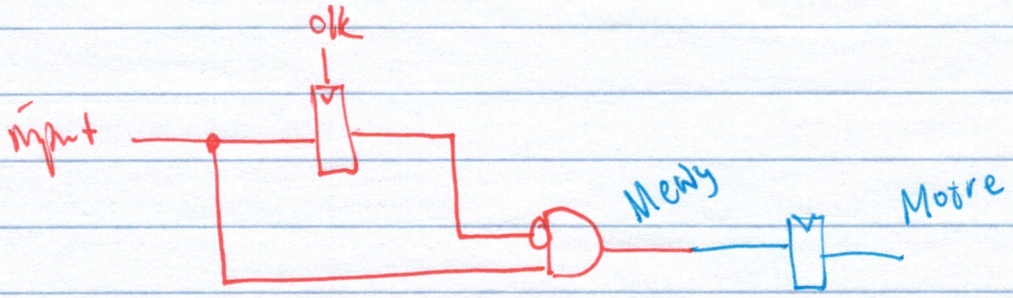
1) Add extra states into FSM

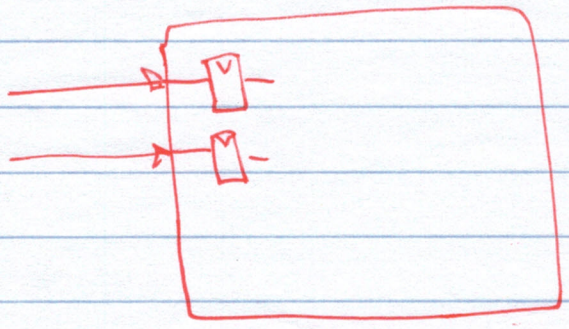


2)

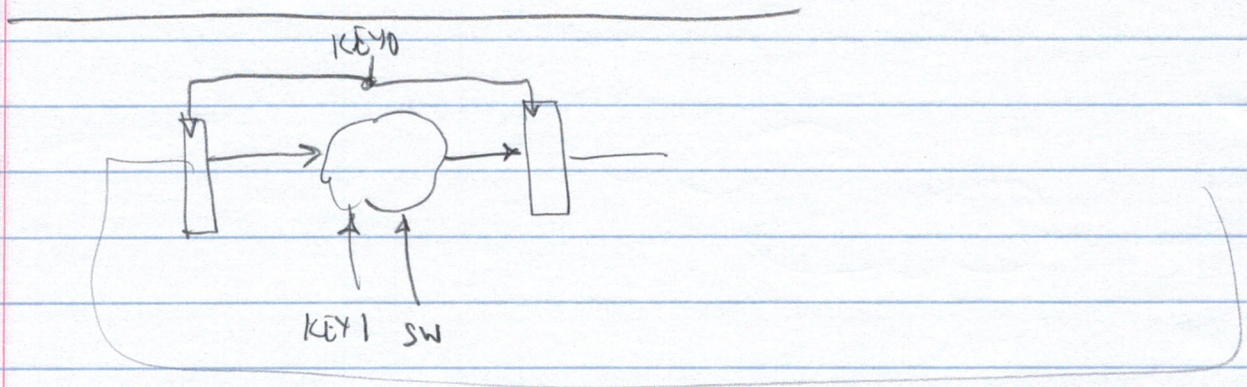


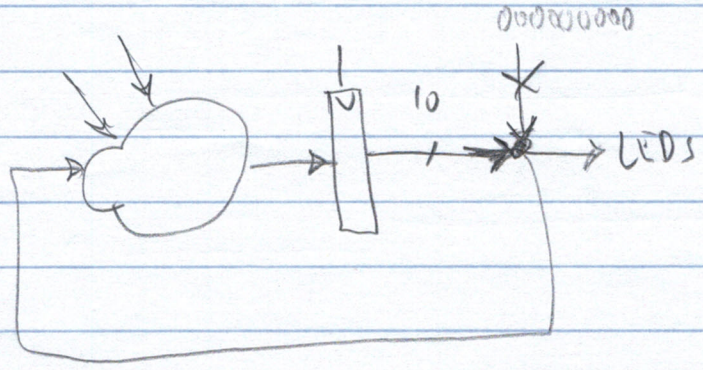






Register all inputs into a block





led = 10'b000 -- 0;