EEC 180

Clocks

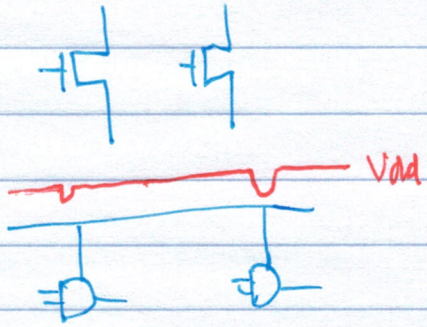
May 4, 2021

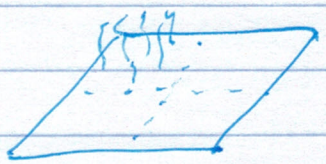
Clocks pace the flow of data inside digital processors

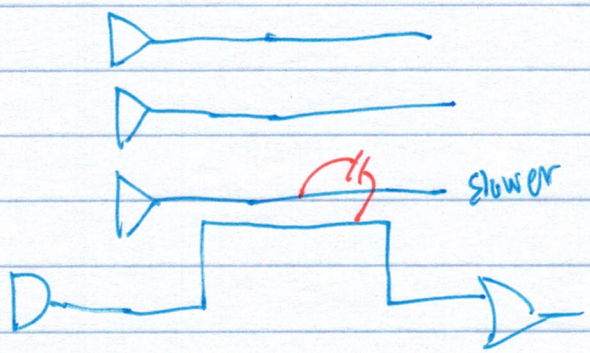
Variations

"PVT"

- Process
- Supply Voltage
- Temperature
- Parasitics, ex. capacitance



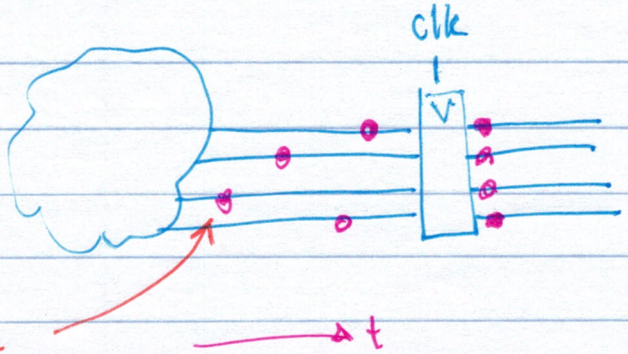


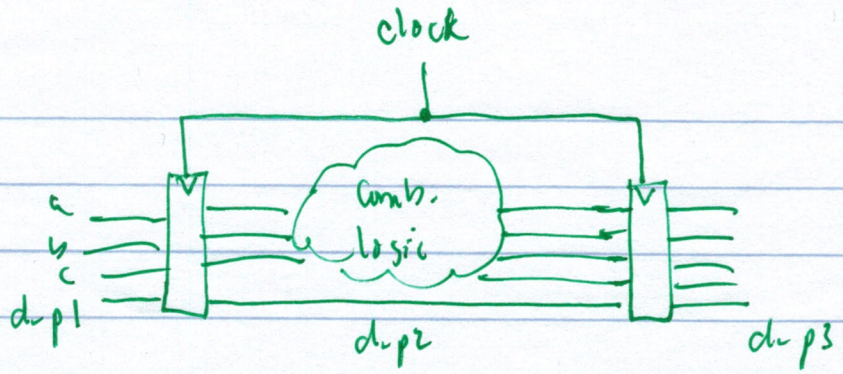


- Data-dependent variations

1 OR 1 = 1 faster

1 OR 0 = 1

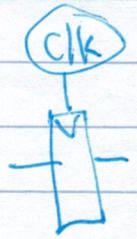




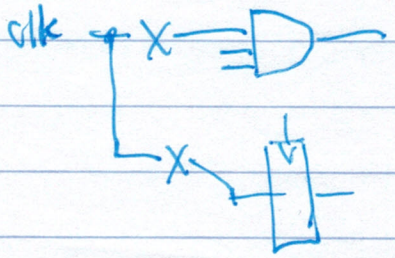
Use FFs

Rules

1) Only clk may connect to clk input of a FF

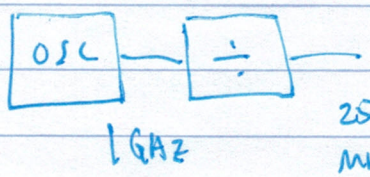


2) clks may not connect to any node other than FF clk input

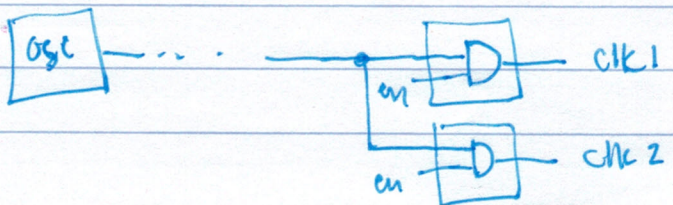


Exceptions:

- Clock generation circuits



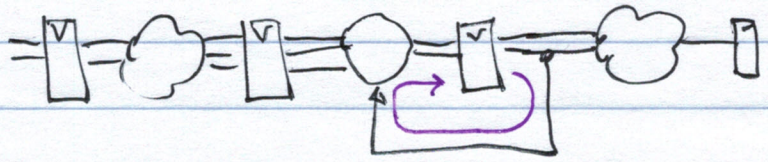
- Clock gate



circuit design issues

180 system
gate =D-
→ circuit +5

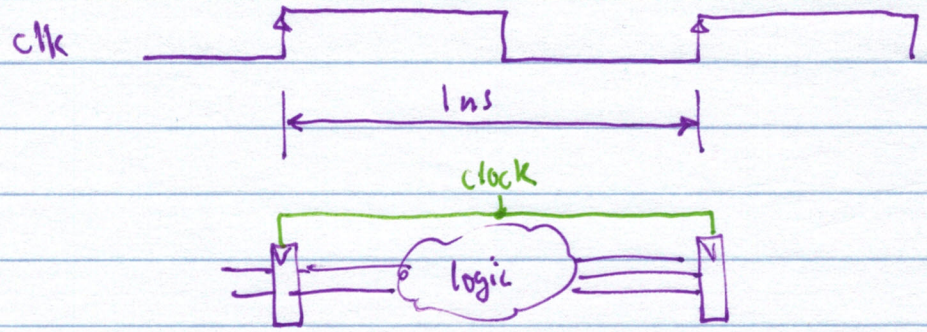
Critical Timing Relationships



Requirement #1 - Logic is not too slow (clock not too fast)

Ex: 1 GHz = 10^9 Hz

clock period = $1/10^9 = 10^{-9}$ sec = 1 nsec

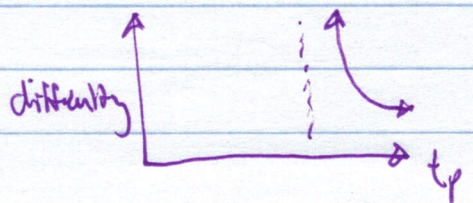


$$t_{clk\text{-}to\text{-}Q} + t_{logic_{max}} + t_{setup} \leq t_{cycle}$$

$$\leq 1/freq$$

What if relationship is violated?

A) Design time
- speed up logic



B) After chip is built

- reduce clk freq

i) Product

a) 4.0 GHz → 3.9 GHz ✓ ok

b) 60 fps → 59.9 fps ✗ fail

ii) Research

6.0 GHz → 5.9 GHz ✓ ok

---

reg out;

case ({a, b})

00: begin out = 1'b0; end

01: 0

10: 0

11: 1

endcase

5'hFF 1 1 1 1 1

5'b11111

X	X	X	X
-8	4	2	1

1 0 0 0 = -8

0 1 1 1 = +7

1 1 1 1 = -1

X	X	X	X
8	4	2	1

0 0 0 0

1 0 0 1 = 9

0-9

1 xxx

0 xxx