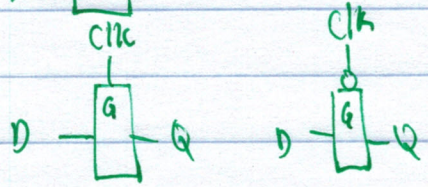
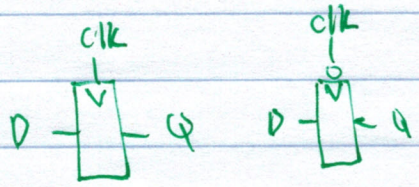
April 22, 2021

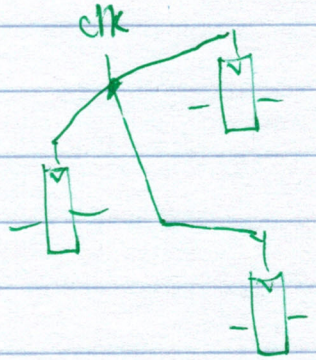
1) Single-Bit Memories

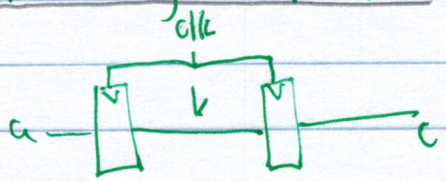
a) 


b) 


* c) FFs 


2) Array

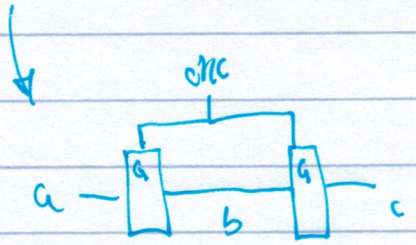
Non-blocking assignment "<=" 

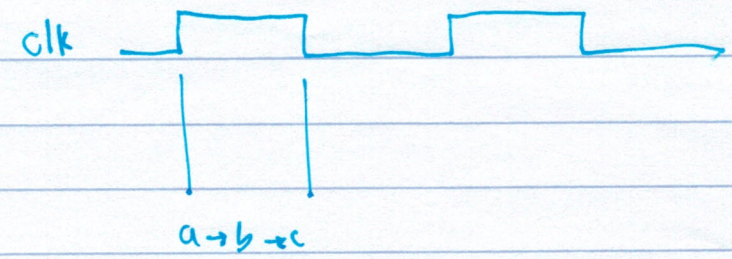



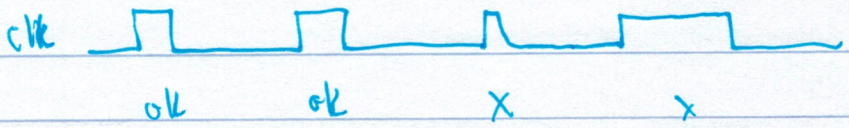

```
reg b, c;
always @(posedge clk) begin
    b <= a;
    c <= b;
end
```

**4 Rules** for memories in RTL

1) Use only FFs, not trans. latches or clock(es) latches

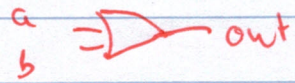



2) For comb. logic always blocks, always use blocking assignment "="

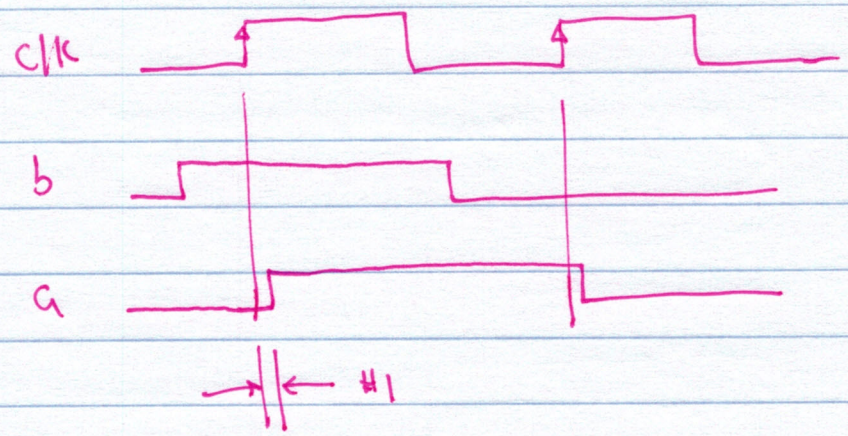
```
// OR
always @(*) begin
    out = a | b;
end
```




3) For FFs always use non-blocking "<="

4) For RTL: Add #1 for clk-to-Q delay

```
always @ (posedge clk) begin
    a <= #1 b;
    Q <= #1 D;
```




5) Guideline

Do not include logic in a FF declaration

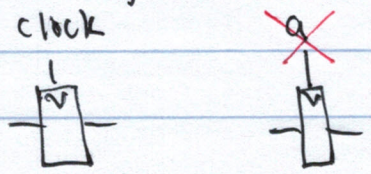
```
always @ (posedge clk) begin
    a <= #1 out;
    x <= #1 y;
    if (reset == 1'b1 && state == 5'h12) begin
        ==
    end
end
```

6) Suggestion

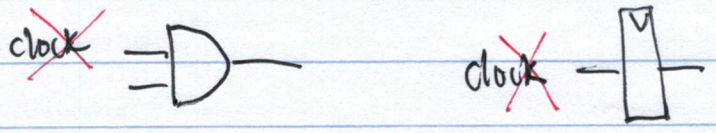
```
// Block 1
// Comb. logic
// FF

// Block 2
// ..
// ..
```

7) a) Only a clock may connect to a FF clock input




b) Clock may not connect to any node other than a FF clock input




c) There are a few exceptions – not in 120