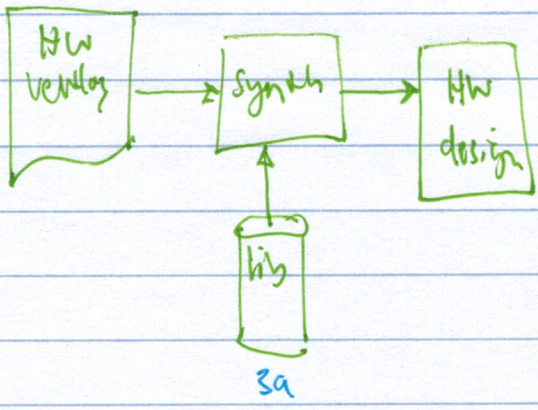
April 13, 2021

Time & Delay

1) Wall clock time

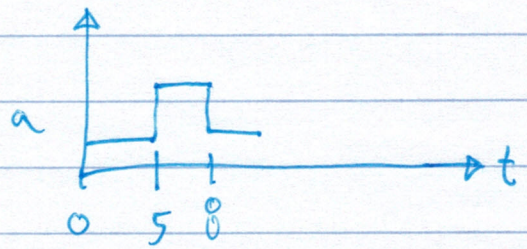
* 2) Time within a simulation
set by "#"



3) Circuit delays
a) ceh lib timing models
b) for Static Timing Analysis
c) t_p found by spice
d) measured silicon

#n // delay on n units

Ex:
```
a = 1'b0;
#5;
a = 1'b1;
#3;
a = 1'b0;
```



Three places for "#" delays
1) Verilog test bench - must be used

2) In a FF declaration (in HW verilog!)
- timing diagrams more readable
- often give a warning
- clock-to-Q delay

3) cell libraries

`timescale time unit base / precision base

↑ #1 delay

Base {s, ms, us, ns, ps, fs}

Ex: `timescale 1ns/10ps

#5 → 5 ns delay

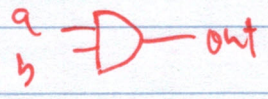
4 Common Mistakes

①
```
wire b;
reg out;
always @(...) begin
    out = x;
    =
    assign b = ...;
end
```

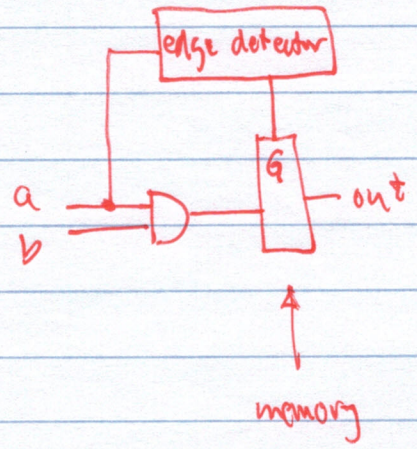
② setting same reg in multiple always blocks

```
always @(posedge clk, negedge reset) begin   // reset
    if (reset == 1'b1) begin
        X <= 1'b0;
end

always @(...) begin
    X <= a + b;
end
```

③ Inferring state in combinational logic w/ an incomplete sensitivity list

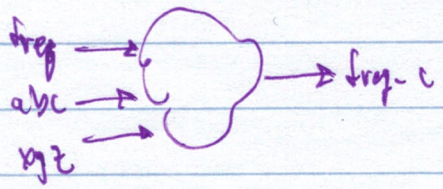



```
reg out;
always @ (a) begin
    out = a & b;
end

always @ (*) begin
```



④ Infer state by not setting a reg in all paths

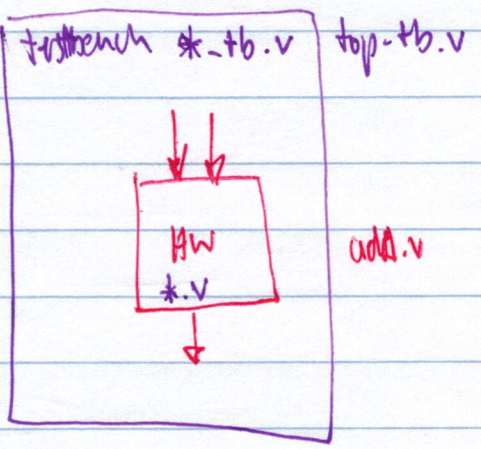
```
always @ (*) begin
    if (xyz == 2) begin
        freq_c = abc;
    end
    =
    case (freq) begin
        3'b000: freq_c = ~~
        3:b001: freq_c = ~~
    endcase
end
```



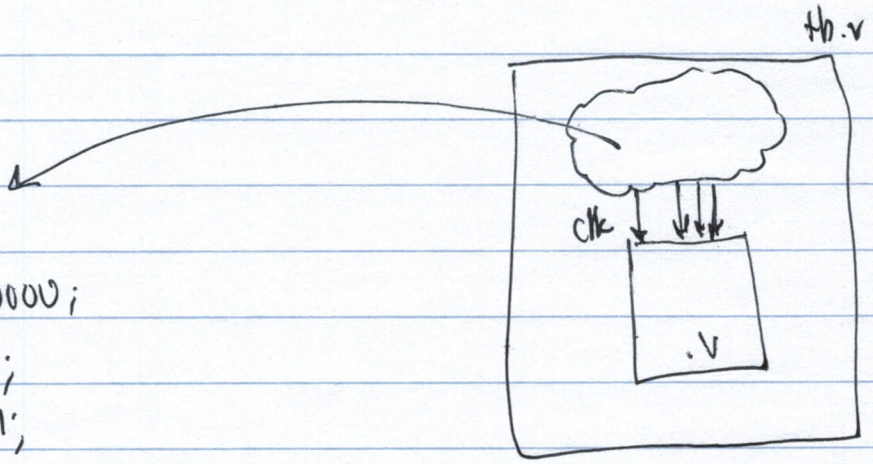
3 fixes: a) add default at beginning of always

Ok for testbench but not Hw

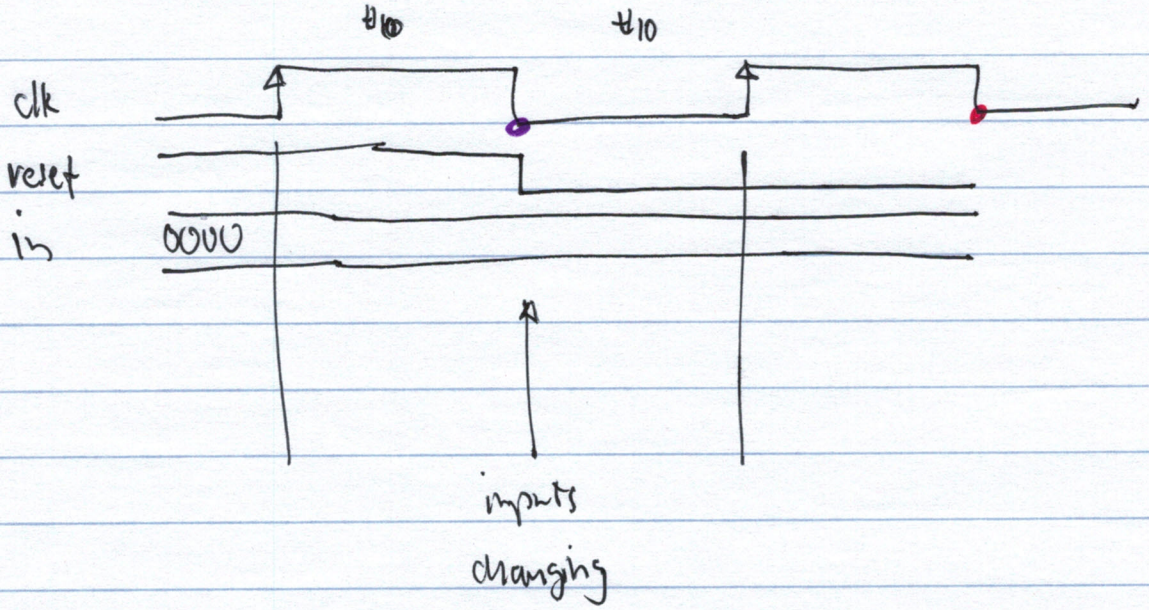
- # delay
- signed reg
  signed wire
- "for" loops
- # write
  # display
- @ (posedge clock)
  @ (negedge clock) } w/o "always"
- repeat (50) @(posedge clock)
- # stop;
  # finish;
- `timescale - first line of top-level testbench



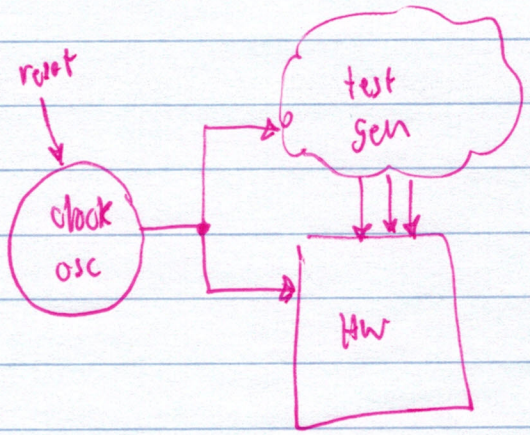
Approach 1

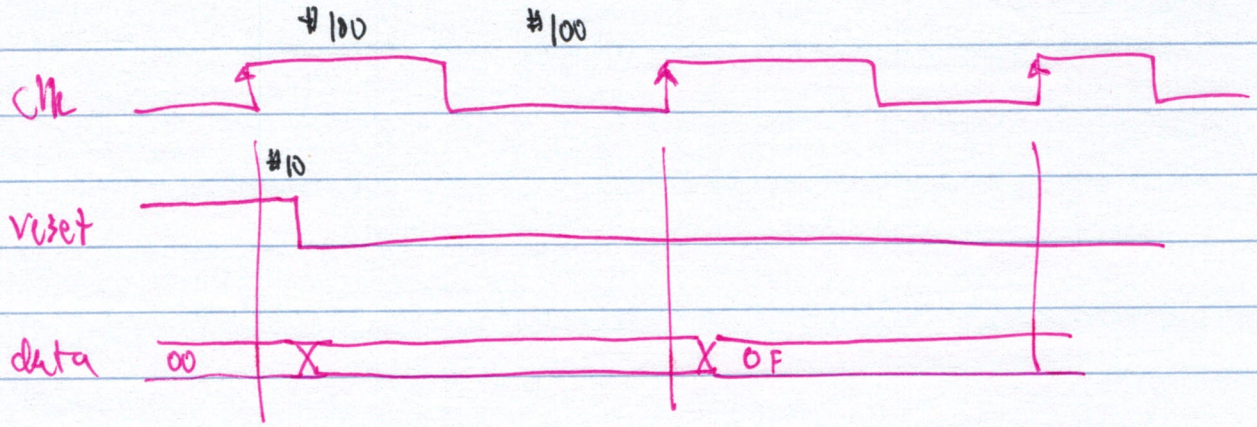



```
initial begin
    in = 4'b0000;
    clk = 1'b0;
    reset = 1'b1;
    #10; clk=1'b1; #10; clk=1'b0;

    reset = 1'b0;
    #10; clk=1'b1; #10; clk=1'b0;

    #stop;
```


#10
#10
clk
reset
in
0000
inputs
changing

Approach 2


reset
test
gen
clock
osc
HW


#100
#100
clk
#10
reset
data
00
X
X
0F