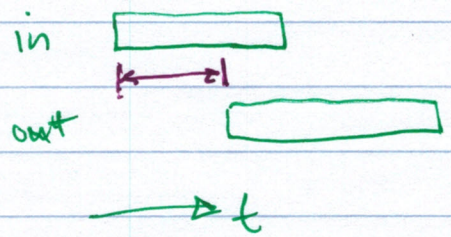
April 1, 2021

Design Metrics

1) Energy per operation
   Ex: Joules per JPEG image compressed

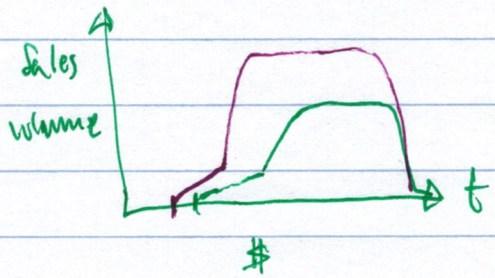
2) Performance
   a) Throughput Ex: 250 MSamples/sec (high) better
   b) Latency time from first data in → ~~last~~ first! data out (low) better



   c) Numerical precision

3) Circuit area (resources)

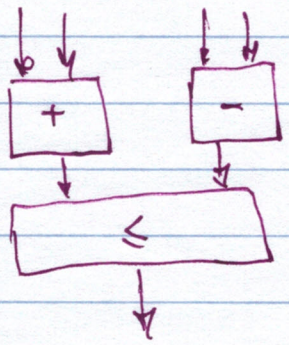
4) Design complexity
   design time → "time to market"



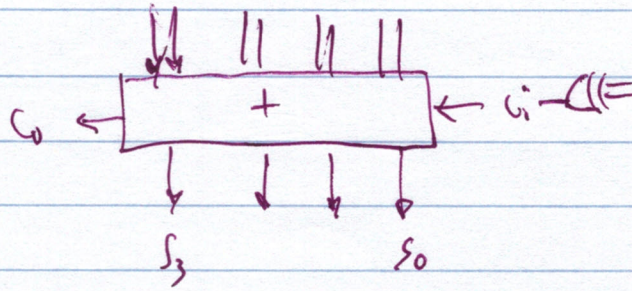
5) Suitable for future fab. technologies ← fabrication
   - More transistors
   - More faults
   ⋮

7 diagrams

1) Block diagram

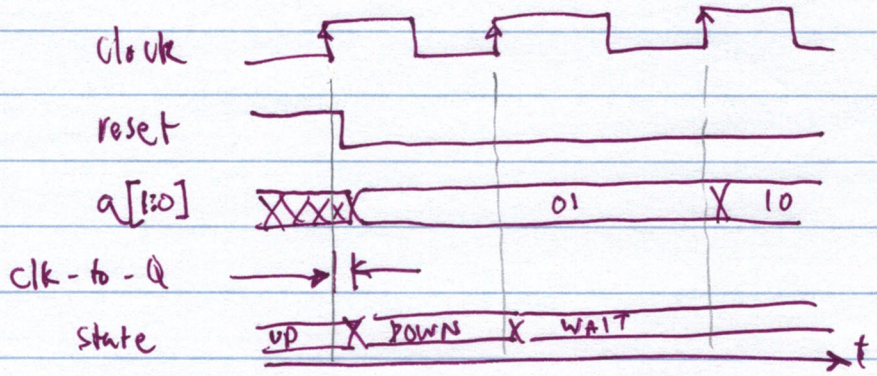


2) Circuit diagram
- more detail than Block

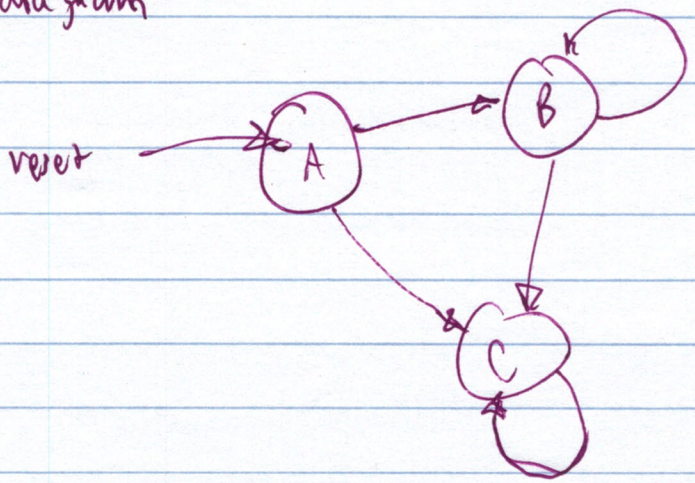


3) Timing

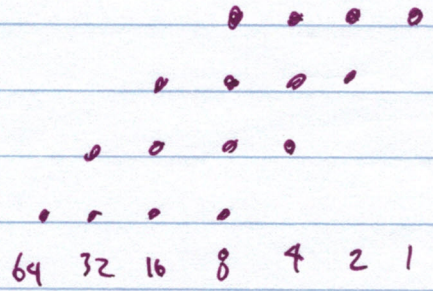
logic level vs. time



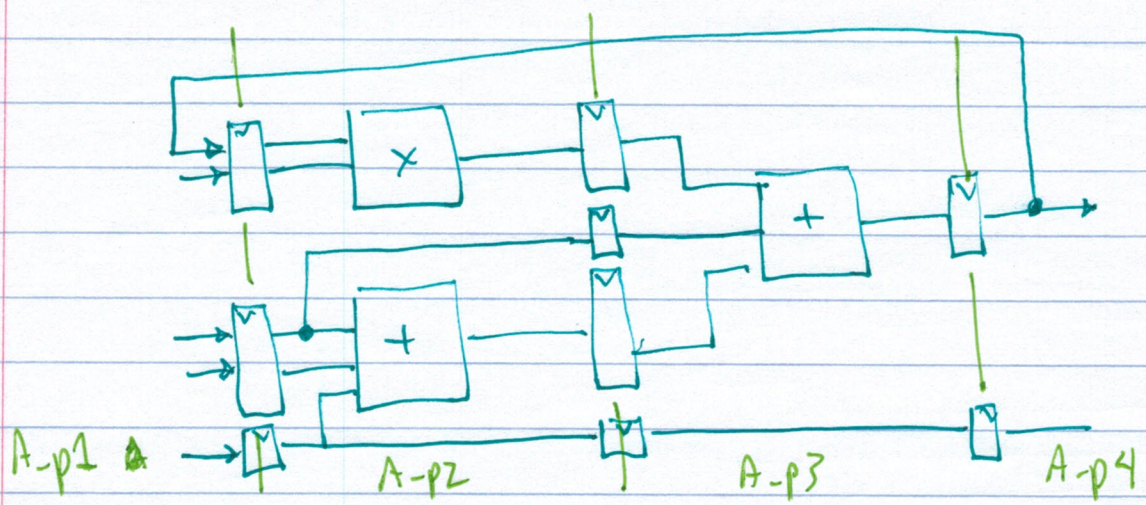
4) State diagram



5) Arithmetic dot diagram

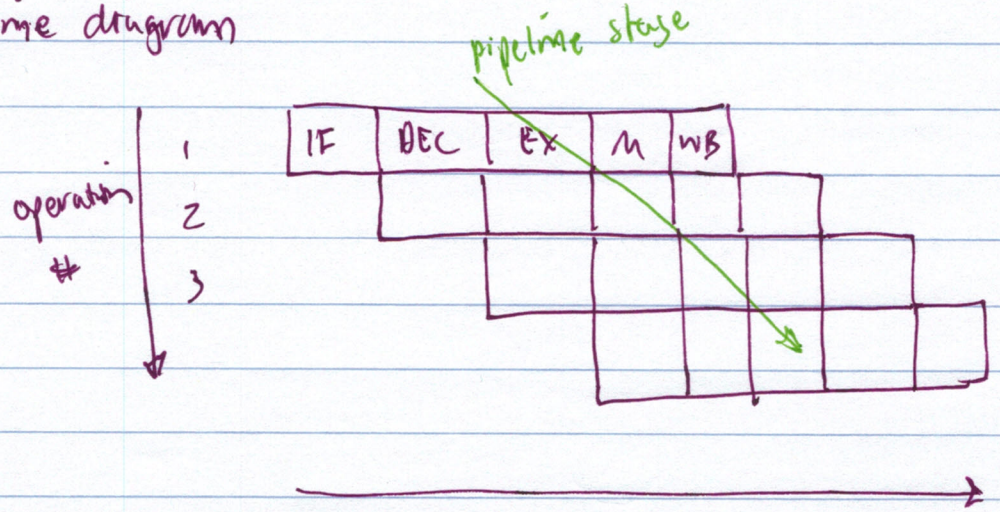


6) Pipelined Block diagram



- All registers aligned
- "Reverse" steering signals need not be registered

7) Pipeline diagram



O.H. Mon 4-5 Apr. 5

Chip Design Methodologies

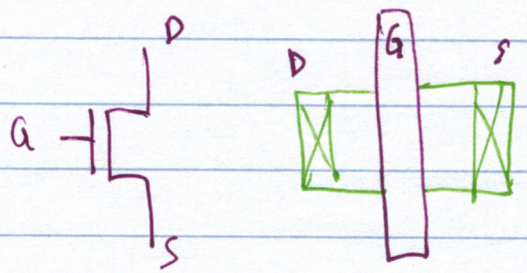
1) Full Custom — $50M one-time cost
   highest perf.
   lowest energy/op.
   lowest cost per part

↕

6) Programmable general purpose
   lowest design time
   lower one-time cost

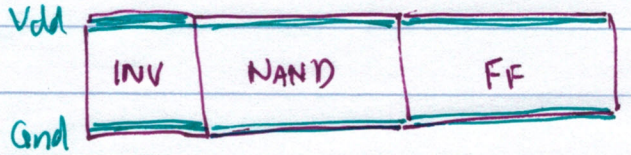
VLSI - Very large Scale Integration
- "semiconductor chip"

1) Full custom



- analog

2) Standard cell
- same height



- can be "Placed & Routed" by computer

3) Gate Array

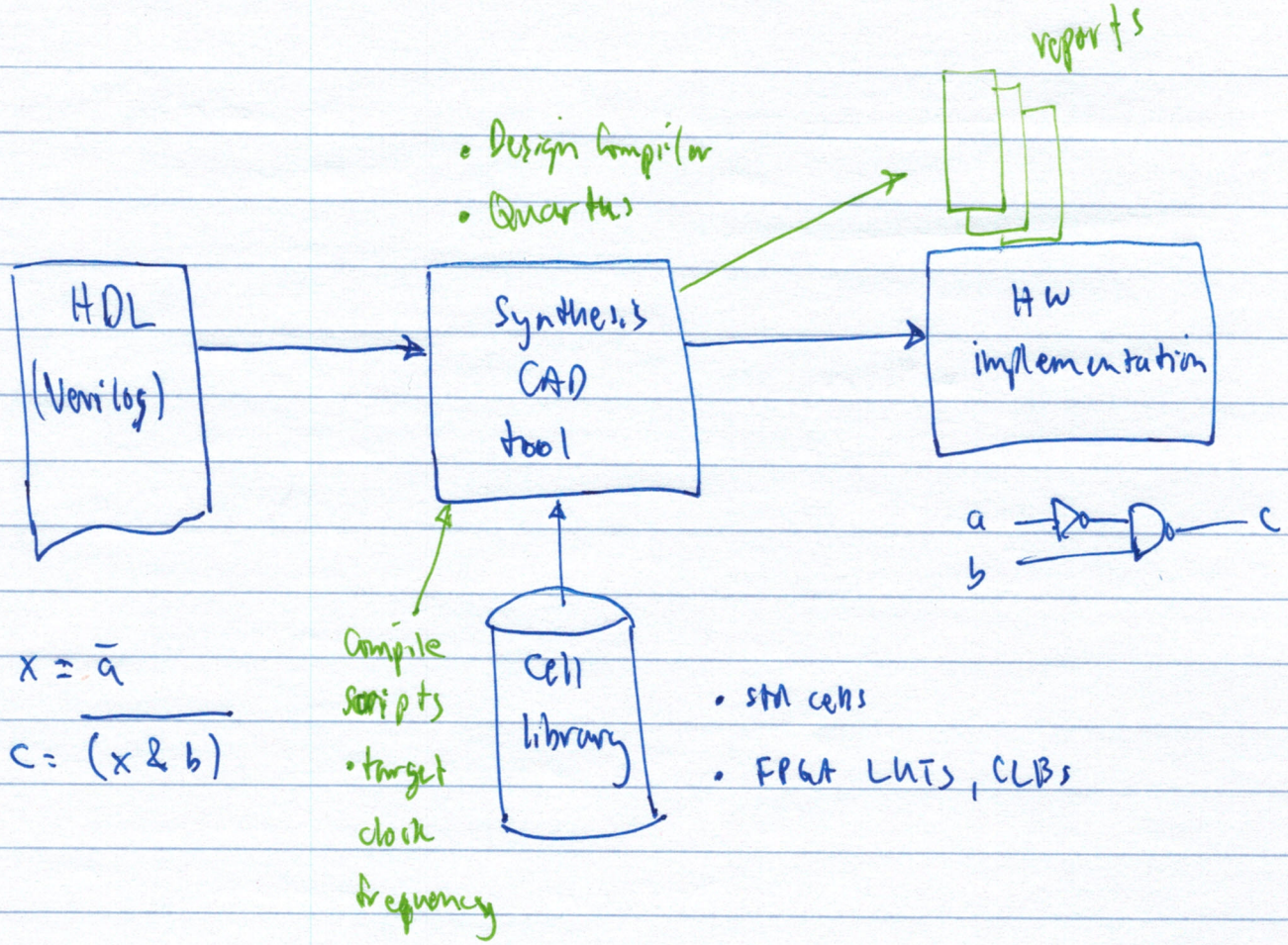
- customized with metal layers

4) Field - Programmable Gate Array - FPGA

- customized with config bits

5) Prog. Special - purpose
- DSP
- GPUs

6) Prog. General - purpose
- Intel
- AMD
- ARM


reports
• Design Compiler
• Quartus
HDL
(Verilog)
Synthesis
CAD
tool
HW
implementation
a
b
c
Compile
scripts
• target
clock
frequency
Cell
library
• std cells
• FPGA LUTs, CLBs

$x = \bar{a}$

$c = (x \,\&\, b)$