7 BASIC DIAGRAMS
1. Block diagram
   - Just like it says; diagram of blocks (and connections)

2. Circuit diagram
   - Often the same as a block diagram
   - In 180, does not require details to the gate level (NAND, NOR, etc.) but it should have more circuit-level detail
3. **Timing diagram**

- Logic level (voltage) versus time
- As a rule, the *clock* is at the top. Draw a small arrow on each active edge. Draw a light vertical line aligned with each active clock edge.
- Several common waveform features:
  - Simple single-bit signal 0/1 values
  - Multi-bit bus
  - Transition location or region where a signal, or signal(s) within a bus, changes value
3. Timing Diagram continued

- Draw transitions of signals that come from a register a very short time after the active edge of the clock, not at the same time as the clock edge.
- Timing diagrams may also show higher-level events such as state and counter values.
4. State Diagram

5. Arithmetic Dot Diagrams

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6. Pipelined Block Diagram

- All registers are aligned with others in the same pipeline stage
- “Reverse-flowing” signals are generally not pipelined
- It is often advisable to include a pipeline notation in the signal name
7. Pipeline Diagram
   - Useful for designing deeply-pipelined digital processors

constant HW pipeline stages

operation number
time

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