FIELD PROGRAMMABLE GATE ARRAYS (FPGAs)

Major Vendor: Xilinx

- Virtex — High end
  16 nm, 20 nm, 28 nm
- Kintex — Balanced cost/performance/energy
  16 nm, 20 nm, 28 nm
- Artix — Low power, Low cost
  28 nm
- Spartan — Low cost
  28 nm, 45 nm

https://www.xilinx.com/products/silicon-devices/fpga.html

Example: Xilinx 7-series

- LUT: Look-Up Table
  - LUTs can implement any arbitrarily-defined 6-input Boolean function
  - Configurable as a 6-input LUT with one output, or two 5-input LUTs with separate outputs but common inputs
- Slice
  - Contains four 6-input LUTs
  - Contains four flip-flops (eight storage elements)
  - Multiplexers and arithmetic carry logic
  - There are two types
- CLB: Configurable Logic Block
  - Each CLB element contains a pair of slices
  - Each CLB connects to a switch matrix for access to the general routing matrix

https://www.xilinx.com/support/documentation/user_guides/ug474_7Series_CLB.pdf

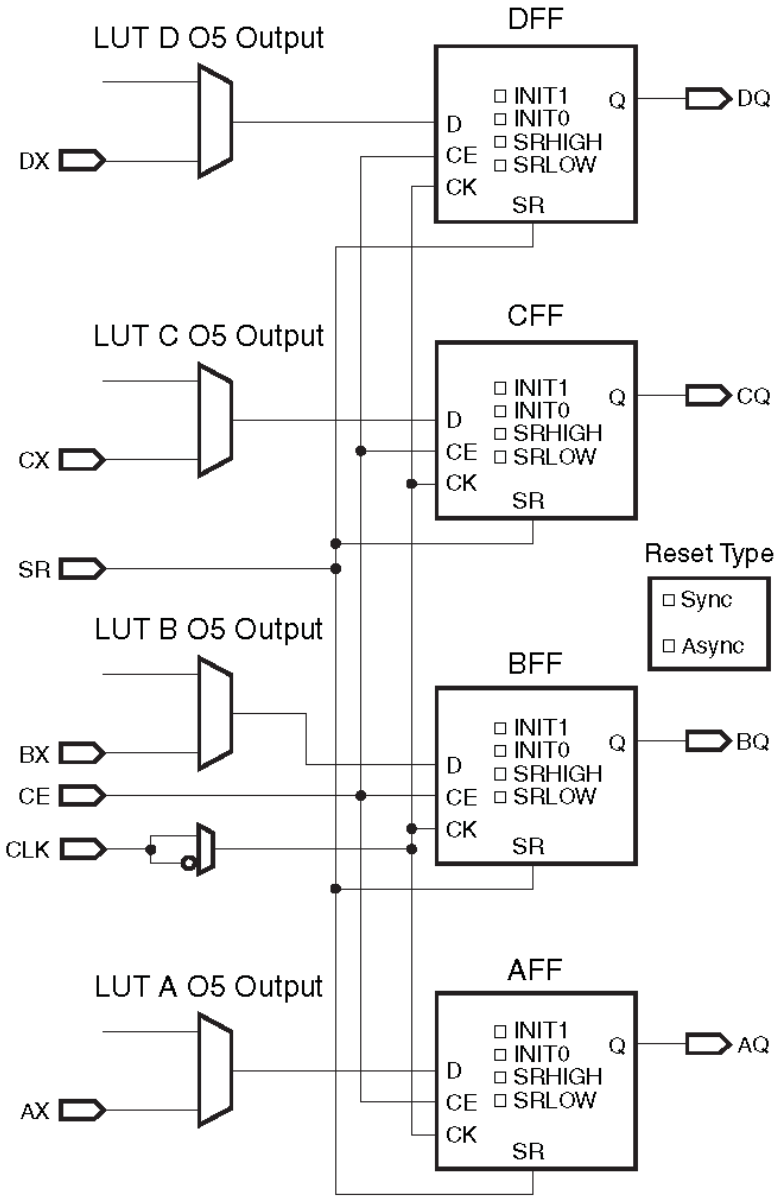
Example: Xilinx 7-series

- Virtex-7 364,200 – **1,221,600** LUTs
- Kintex-7 41,000 – 298,600 LUTs
- Artix-7 8000 – 134,600 LUTs
- Spartan-7 **3752** – 64,000 LUTs

https://www.xilinx.com/support/documentation/user_guides/ug474_7Series_CLB.pdf

Example: Xilinx 7-series

- An example configuration of a Xilinx series-7 slice
  - Four flip-flops are DFF, CFF, BFF, AFF
  - Flip-flops can be configured for synchronous or asynchronous set or reset
  - LUTs are not shown; their outputs enter the slice on the right of the diagram



https://www.xilinx.com/support/documentation/user_guides/ug474_7Series_CLB.pdf

Major Vendor: Altera/Intel

- Stratix — Highest performance
- Arria — Balanced cost, power, performance
- Cyclone — Low cost
- Max — Non-volatile single-chip
  - Our DE10-Lite board uses a MAX 10 10M50DAF484C7G device
  - https://www.altera.com/products/fpga/max-series/max-10/overview.html

MAX® 10

INTEL® MAX® 10 FPGAS PRODUCT TABLE

PRODUCT LINE		10M02	10M04	10M08	10M16	10M25	10M40	10M50
LEs (K)		2	4	8	16	25	40	50
Block memory (Kb)		108	189	378	549	675	1,260	1,638
User flash memory[1] (KB)		12	16 – 156	32 – 172	32 – 296	32 – 400	64 – 736	64 – 736
18 x 18 multipliers		16	20	24	45	55	125	144
Phase-locked loops (PLLs)[2]		1, 2	1, 2	1, 2	1, 4	1, 4	1, 4	1, 4
Internal configuration		Single	Dual	Dual	Dual	Dual	Dual	Dual
Analog-to-digital converter (ADC), temperature sensing diode (TSD)[3]		-	1, 1	1, 1	1, 1	2, 1	2, 1	2, 1
External memory interface (EMIF)		Yes[4]	Yes[4]	Yes[4]	Yes[5]	Yes[5]	Yes[5]	Yes[5]
Package Options and I/O Pins: Feature Set Options, GPIO, True LVDS Transceiver/Receiver								
V36 (D)[6]	WLCSP (3 mm, 0.4 mm pitch)	C, 27, 3/7	–	–	–	–	–	–
V81 (D)[7]	WLCSP (4 mm, 0.4 mm pitch)	–	–	C/F, 56, 7/17	–	–	–	–
F256 (D)	FBGA (17 mm, 1.0 mm pitch)	–	C/A, 178, 13/54	C/A, 178, 13/54	C/A, 178, 13/54	C/A, 178, 13/54	C/A, 178, 13/54	C/A, 178, 13/54
U324 (D)	UBGA (15 mm, 0.8 mm pitch)	C, 160, 9/47	C/A, 246, 15/81	C/A, 246, 15/81	C/A, 246, 15/81	–	–	–
F484 (D)	FBGA (23 mm, 1.0 mm pitch)	–	–	C/A, 250, 15/83	C/A, 320, 22/116	C/A, 360, 24/136	C/A, 360, 24/136	C/A, 360, 24/136
F672 (D)	FBGA (27 mm, 1.0 mm pitch)	–	–	–	–	–	C/A, 500, 30/192	C/A, 500, 30/192
E144 (S)[6]	EQFP (22 mm, 0.5 mm pitch)	C, 101, 7/27	C/A, 101, 10/27	C/A, 101, 10/27	C/A, 101, 10/27	C/A, 101, 10/27	C/A, 101, 10/28	C/A, 101, 10/28
M153 (S)	MBGA (8 mm, 0.5 mm pitch)[8]	C, 112, 9/29	C/A, 112, 9/29	C/A, 112, 9/29	–	–	–	–
U169 (S)	UBGA (11 mm, 0.8 mm pitch)	C, 130, 9/38	C/A, 130, 9/38	C/A, 130, 9/38	C/A, 130, 9/38	–	–	–

Notes:
1. Additional user flash may be available, depending on configuration options.
2. The number of PLLs available is dependent on the package option.
3. Availability of the ADC or TSD varies by package type. Smaller pin-count packages do not have access to the ADC hard IP.
4. SRAM only.
5. SRAM, DDR3 SDRAM, DDR2 SDRAM, or LPDDR2.
6. "D" = Dual power supply (1.2 V/2.5 V), "S" = Single power supply (3.3 V or 3.0 V).
7. V81 package does not support analog feature set. 10M08 V81 F devices support dual image with RSU.
8. "Easy PCB" utilizes 0.8 mm PCB design rules.
9. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.altera.com.

C, 27, 3/7 — Indicates feature set options, GPIO count, and LVDS transmitter or receiver count. Feature set options: C = Compact (single image), F = Flash (dual image with RSU), A = Analog (analog features block). Each has added premiums.

Indicates pin migration.

FPGA Chip

- Max 10 10M50DAF484C7G chip
- Light-blue rectangles: Logic Array Blocks (LAB), each of which contains 16 logic elements (LE), each of which contains a 4-input LUT, a flip-flop, and routing muxes
- White rectangles: hardware 18x18 multipliers
  - 144 on each chip
- Yellow rectangles are M9K memory blocks
  - 182 on each chip
  - Total of 182 KBytes (204 KB)
- Green rectangle: on-board flash memory that can store the bit-stream that programs the FPGA when it is powered on
- Brown blocks on the border are I/O ports and drivers