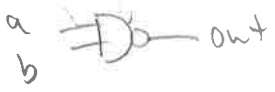
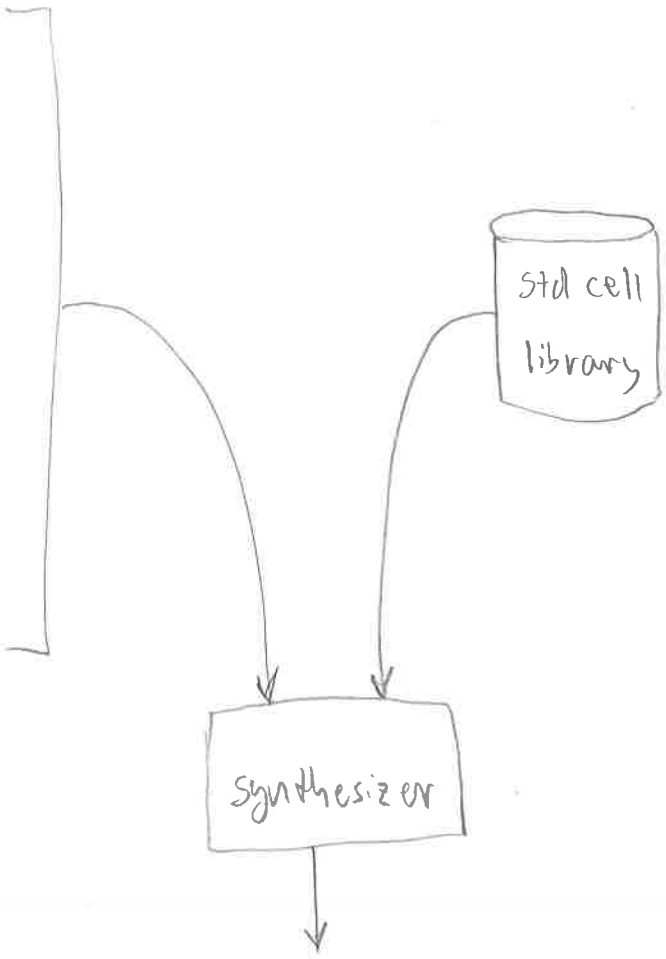
Example: 2-input NAND gate w/ reg

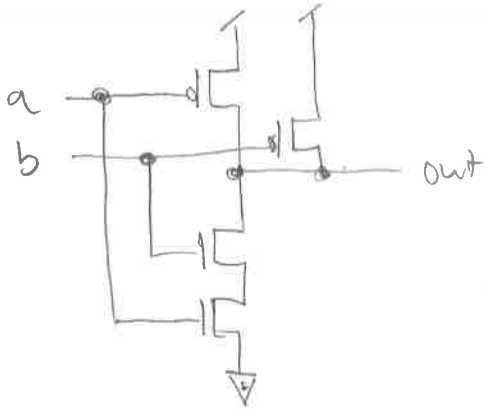


a	b	out
0	0	1
0	1	1
1	0	1
1	1	0

```
// verbose example code
reg out;
always @ (a or b) begin
    out = 1'b1;
    if (a == 1'b1) begin
        if (b == 1'b1) begin
            out = 1'b0;
        end
    end
end
```

in order





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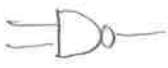

no ordering whatsoever