3) Pseudo-variable-frequency: Clock all logic with the highest-rate clock
   - Utilize simple counters that load registers or route signals on only certain clock edges (for example, every fourth clock edge for \( \text{freq}/4 \)).
   + Definitely the simplest and most robust
   - Counters must be reset simultaneously and the \textit{reset} signal must meet timing requirements at the highest frequency
   • Design in only this way in this class when variable frequency is needed
Effectively Dividing the Frequency of a Clock

- Example of effectively dividing a clock by a factor of 256 using an 8-bit counter `count`

```
clock
11111101  11111110  11111111  00000000  00000001

count
11111101  11111110  11111111  00000000  00000001

enable_reg
```