Critical Timing Relationships

If these are violated, the circuit will definitely fail under some circumstances.

Fundamental block of every clocked digital system:

- FSM control, datapath, anything
- could also use latches, but we use FFs

- could be the same register for both sides
Requirement #1: Logic is not too slow (clock not too fast)

Ex: 1 GHz clock

\[ \text{clock period} = \frac{1}{\text{freq}} = \frac{1}{10^9 \text{ Hz}} = 10^{-9} \text{ sec} = 1 \text{ nsec} \]

- There is one clock period for data to get from one register to the next one.
  a) clock edge → Q output
  b) time for the slowest path through the comb. logic
  c) time to arrive before the active clock edge

"time circuit requires ≤ time allowed, for correct operation"

\[ t_{\text{clk-to-a}} + t_{\text{logic max}} + t_{\text{setup}} \leq t_{\text{cycle}} \leq \frac{1}{\text{freq}} \]
What if the requirement is violated?

A) Design time
   - speed up logic
   but...

B) After chip is built
   - only torque is available
     slow f_{ck} → longer torque
     i) product - maybe ok
        1.9 GHz proc instead of 2.0 GHz ✓
        59 frames per second vs. 60 fps x
     ii) research - probably fine
Egnation assumes clocks are perfectly aligned.

What if clk2 is 0.1 ns late compared to clk1 and clk3?

\[ t_{\text{cycle A}} = 1.0\text{ns} + 0.1\text{ns} = 1.1\text{ns} \]

\[ t_{\text{cycle B}} = 1.0\text{ns} - 0.1\text{ns} = 0.9\text{ns} \]

\[ t_{\text{cycle avail}} = \frac{1}{\text{freq}_{\text{clk}}} - t_{\text{clk skew worst case}} \]
Requirement #2: Logic is not too fast

Enabled by clock skew which is the difference in arrival times between clock signals.

This failure occurs when the second downstream clock is late w.r.t. to the first upstream clock.
Timing violations make function fail or unreliable

- Race through in worst case

\[ t_{clk-to-a} + t_{logic\ min} > t_{clk-skew} + t_{hold} \]

What if the requirement is violated?

4) Design time
   - lower clock skew
   - increase \( t_{logic\ min} \)

Very easy!
Add slow circuits
B) After chip is built

- no terms are a function of clock

- no fixes possible!

HOLD time violations are very dangerous!