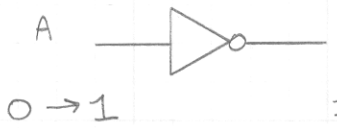
8.3 Gate Delays and Timing Diagrams

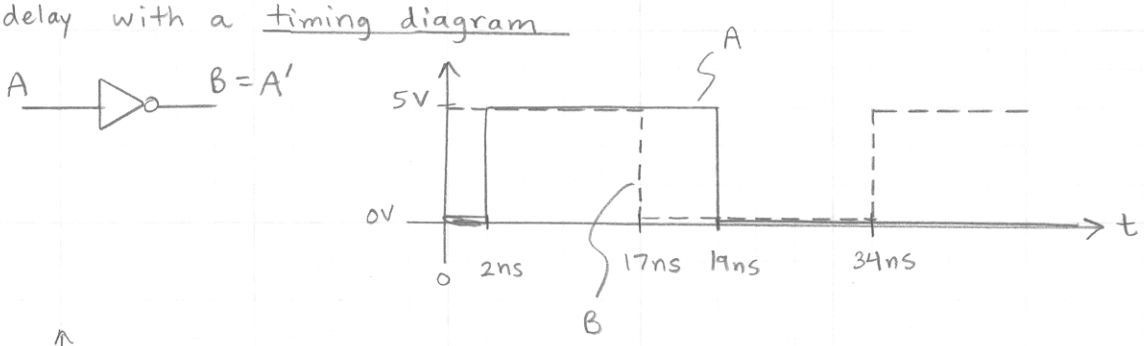
In "steady state" (after "enough" time), logic gate outputs will reach a fixed final value. However, it takes some time to get there.

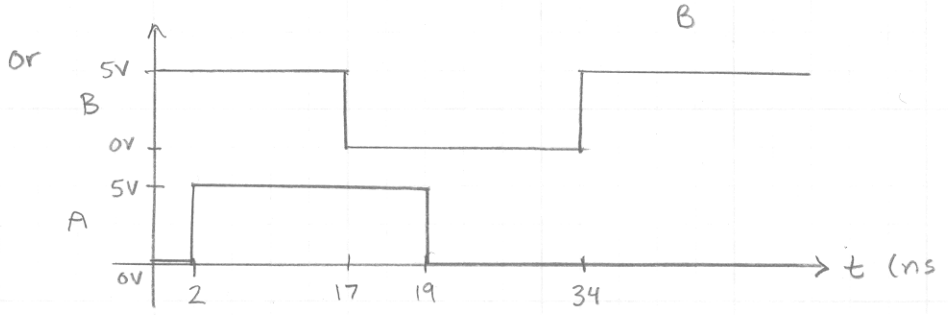


About 15 ns max for 74LS04 parts for output to change after input changes
⇒ propagation delay

Propagation delay for fastest modern chips ~30ps – 40 ps (trillionths of a second).

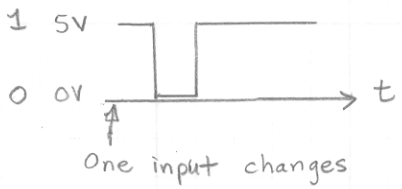
Show delay with a timing diagram



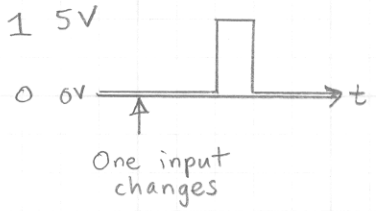


8.4 Hazards in Combinational Logic

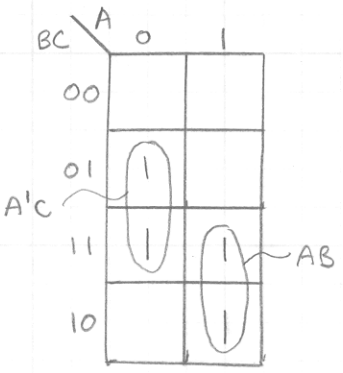
Static 1 Hazard exists in a logic circuit if its output is 1, momentarily goes to 0, then returns to settle at 1 when a single input changes:



Static 0 Hazard output momentarily transitions to 1 when initially 0 and finally settling at 0:



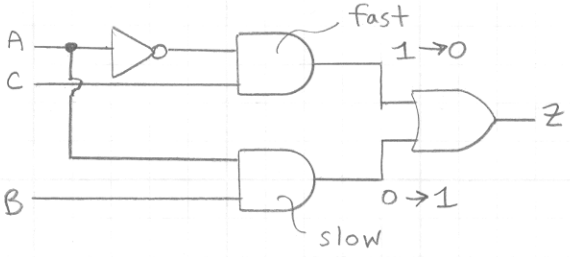
Ex: Static 1 Hazard

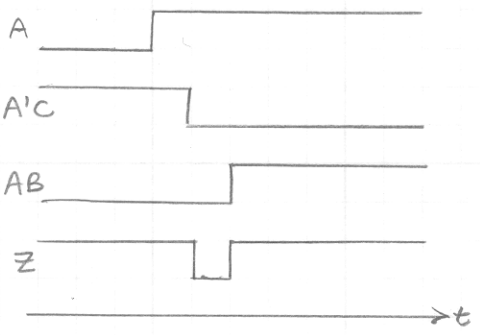


Transition A: 0 → 1

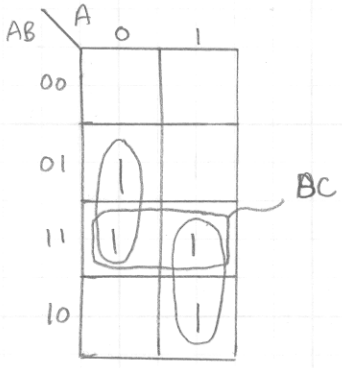
	A	B	C
t ↓	0	1	1
	1	1	1

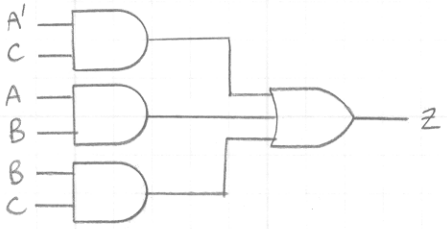
$Z = A'C + AB$





Solution: add redundant gates





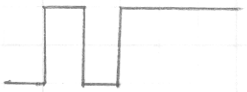
Note: No longer a minimum solution.

Fix hazards by covering all adjacent 1's with their own group.

There will be no static 1 or 0 hazards within a group.

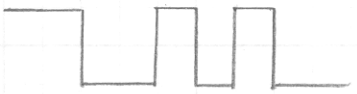
Dynamic Hazards occur when an output makes additional (three or more) transitions when it is expected to transition from 0→1 or 1→0.

Ex:



0 → 1

Ex:



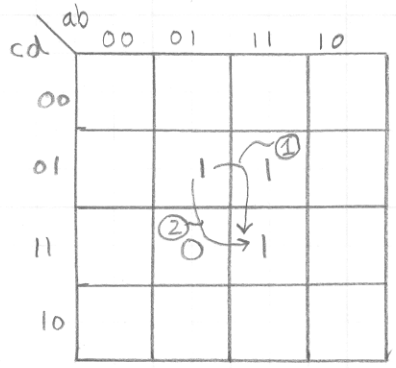
1 → 0

Dynamic hazards occur with multi-level circuits where there are multiple paths from inputs to outputs.

Methods to fix static and dynamic hazards work only for single bit input transitions.

Fix dynamic hazards with static-hazard-free 2-level circuits.

Ex: Multiple input bit transitions.



Transition from abcd = 0101 to abcd = 1111

Case ①

	a	b	c	d	f (output)
	0	1	0	1	1
t ↓	1	1	0	1	1
	1	1	1	1	1

No hazard!

case ②

	a	b	c	d	f
	0	1	0	1	1
t ↓	0	1	1	1	0
	1	1	1	1	1

Static 1 Hazard Unavoidable!

Some other names for possible bugs:

Glitch is an unnecessary (usually unwanted) pulse at the output of a combinational logic circuit (e.g., static 0, static 1 hazards)

Runt pulse is a brief transition that doesn't reach all the way to a valid logic level for 1 or 0

Ex: +5V

Ex: +5V