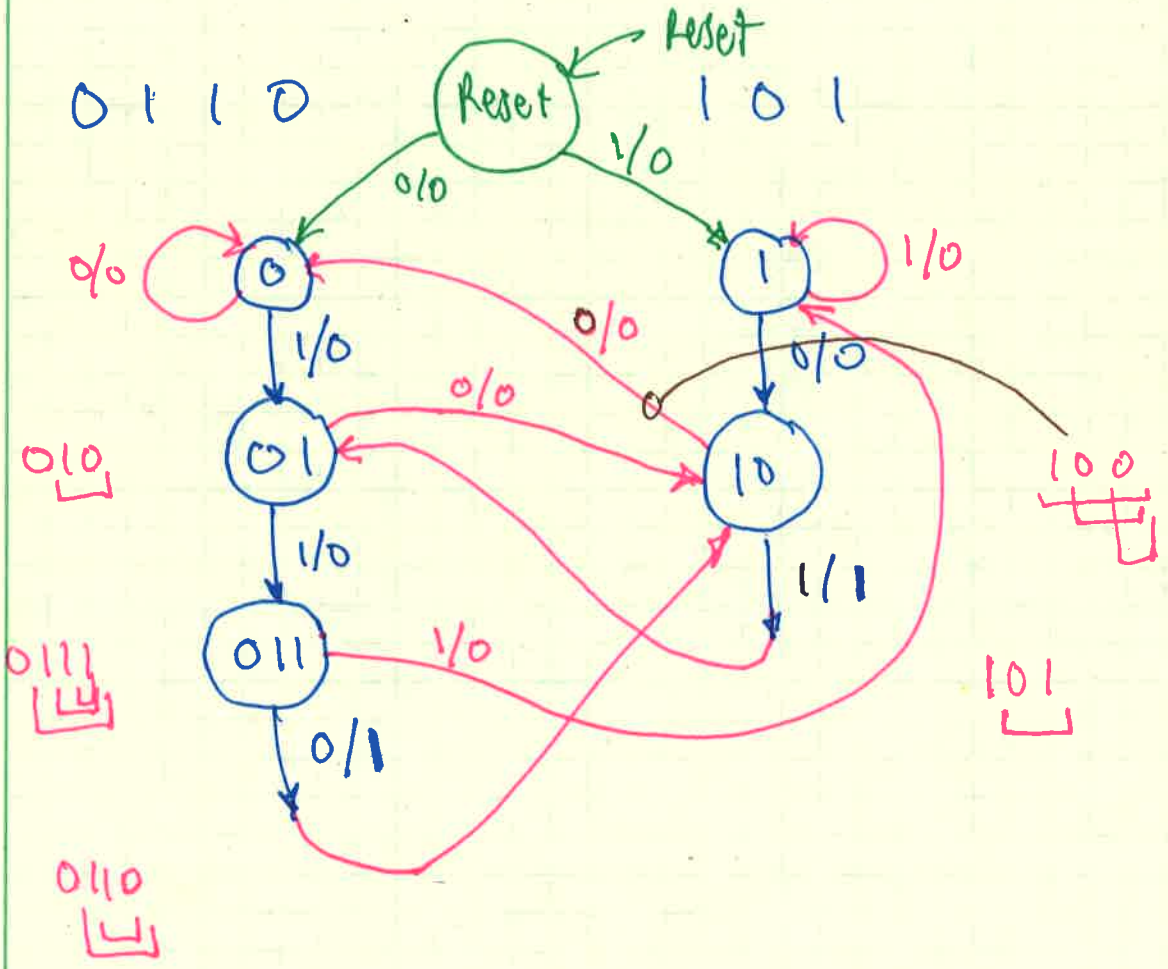
Ex: Sequence Detector

...0110 = X ...101 = X

...0001 = Z ...001 = Z

X = 0 1 0 1 1 0 1

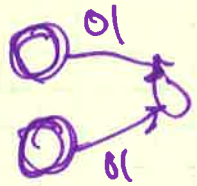
Z = ..0 0 0 1 0 1 1



	P.S.	N.S. $x=0$	N.S. $x=1$	output $x=0$	output $x=1$
S_0	"begin"	"0"	"1"	0	0
S_1	"0"	"0"	"01"	0	0
S_2	"01"	"10"	"011"	0	0
S_3	"011"	10	1	1	0
S_4	"1"	10	1	0	0
S_5	"10"	"0"	"01"	0	1

- DFFs
- Mealy
- # of FFs = $\lceil \log_2(6) \rceil = 3$

Guideline I



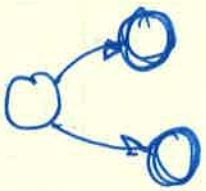
✓ $(S_0, S_1, S_3) \rightarrow$ N.S. S_1 for $x=0$

✓ $(S_2, S_3, S_4) \rightarrow$ " S_3 " $x=0$

✓ $(S_0, S_3, S_4) \rightarrow$ N.S. S_4 for $x=1$

✓ $(S_1, S_5) \rightarrow$ N.S. S_2 for $x=1$

Guideline II



S_0 : S_1, S_4

✓ S_1 : S_1, S_2

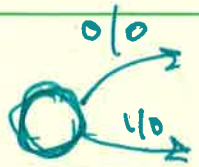
S_2 : S_5, S_3

✓ S_3 : S_5, S_4

✓ S_4 : S_5, S_4

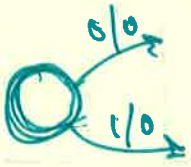
✓ S_5 : S_1, S_2

Guideline III



$S_0, S_1, S_2, S_4 \rightarrow Z=0$ always

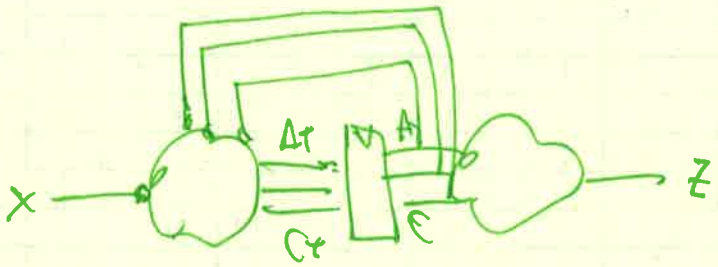
$X = 0, 1$



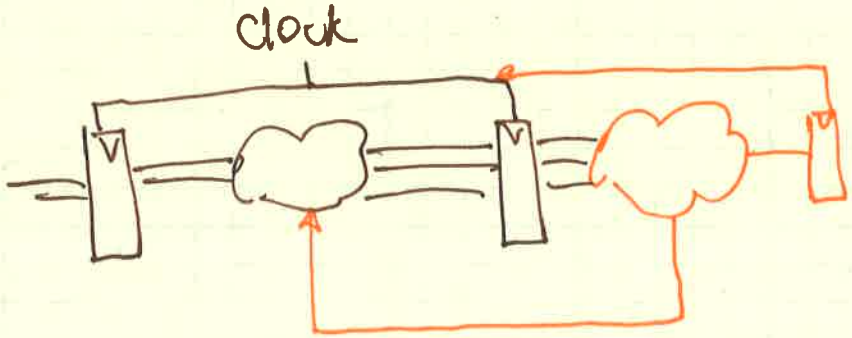
$S_0, S_1, S_2, S_4, S_5 \rightarrow Z=0$ for $X=0$

$S_0, S_1, S_2, S_3, S_4 \rightarrow Z=0$ for $X=1$

- Reset = 000
-

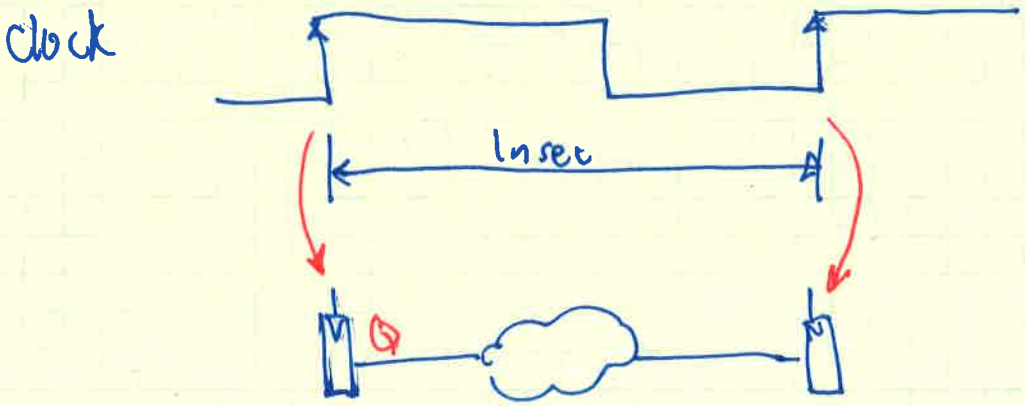


Critical Timing Relationships



Requirement #1 "logic is not too slow" (clock not too fast)

$$\text{clock period} = \frac{1}{\text{freq}} = \frac{1}{10^9\ \text{Hz}} = 10^{-9}\ \text{sec} = 1\ \text{nsec}$$



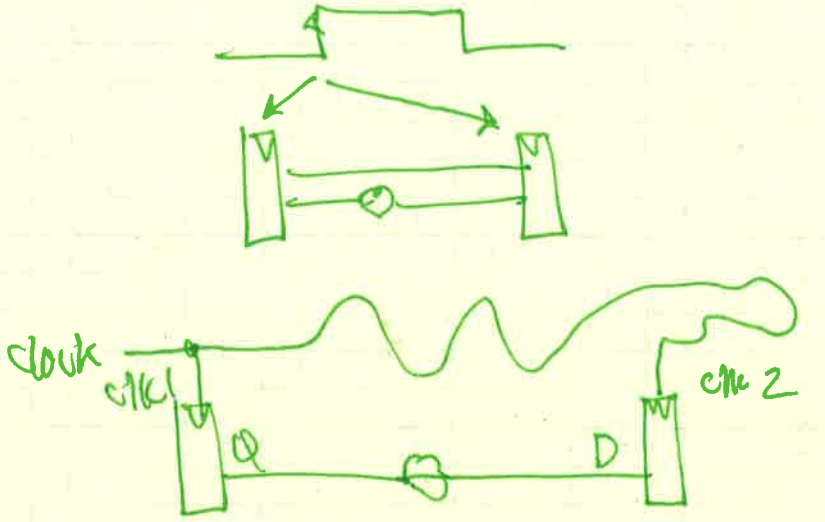
a) clock edge → Q output $t_{clk\text{-}to\text{-}Q}$

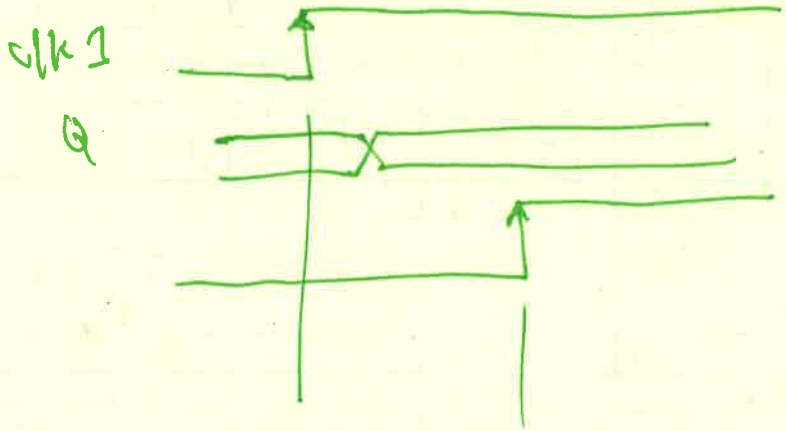
b) logic delay t_{logic} max

c) early at D ff t_{setup}

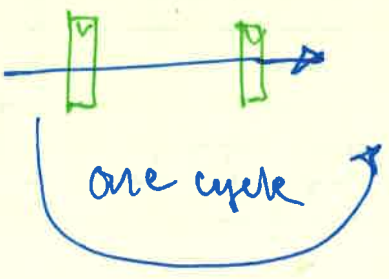
$$t_{clk\text{-}to\text{-}Q} + t_{logic\ max} + t_{setup} \leq t_{cycle} \leq 1/f_{req}$$

Requirement #2 Logic is not too fast, clock not too skewed





- Hold time violation
- Race through



$$t_{clk\text{-}to\text{-}q} + t_{logic_{min}} + t_{wire} > t_{clk\text{-}skew} + t_{hold}$$

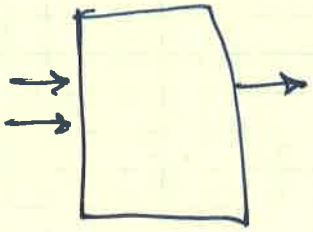
for correct operation

HDL

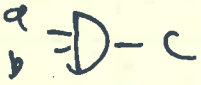
1) Verilog * 18D, 18I, 28I, ...

2) VHDL

1) module

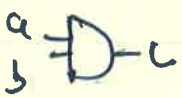


2) wire



```
wire c;
assign c = a & b;
```

3) reg



```
reg c;
always @(a or b) begin
    c = a & b;
end
```