A) Design time
   - speed up logic difficult

B) After chip is built
   - t_cue-to-e, t_logic, t_setup
     can not change
   - can change f_cue
     i) commercial product - maybe ok
        - rebrand at lower clock
        - real-time e.g. 60 fps, 59.9 fps not ok
     ii) research
        - probably ok
Equation 4.1 assumes are aligned

clock: \( f = 1 \text{GHz}, \text{cycle} = 1 \text{ns} \)

clock 1

clk 2

clk 3

For simple analysis,

\[
\text{t}_{\text{cycle available}} = \frac{1}{f_{\text{clk}}} - t_{\text{clk skew max case}}
\]
Requirement #2 (logic is not too fast)

Enabled by clk skew

Happen:

- clock clk1 early
- clk2 late

- hold time violation
- failure, strong wire violation
- race through both stages. Failure
\[ t_{	ext{elec-paq}} + t_{\text{logic min}} > t_{\text{clk-skew}} + t_{\text{hold}} \] for correct operation

What if requirement is violated?

A) Design time
   - Increase \( t_{\text{logic min}} \)
     - Very easy!
     - Add two inrs (slow ones)

B) After chip is built
   - Can not change
   - (no fix turn)
   - No fix is possible

\[ \vdots \text{Hold time violations are very dangerous!} \]
Hardware Description Languages

1) Verilog
   - industry
   - similar to C

2) VHDL
   - govt

SW - code an algorithm

HDL - code HW

Verilog

• Module

• wire - assign

\[
\begin{align*}
& a \rightarrow D \rightarrow c \\
& b \rightarrow D \\
wire \ c; \\
assign \ c = a \& c;
\end{align*}
\]


* reg - always block

```
\[
\begin{align*}
    a & \rightarrow D & d \\
    b & \rightarrow & \\
\end{align*}
\]
```

```verilog
reg d;

always @(a or b) begin
    d = a & b;
end
```

```
clk
D \rightarrow Q
```

```verilog
reg Q;

always @ (posedge clk) begin
    Q = D;
end
```

---

![Verilog block diagram with gate netlist and library](image)
Adders

1) Ripple-Carry

- simplest
- slowest
- smallest

2) Carry-Select Adder

Sum
Multiplication

\[ \begin{array}{c}
110_2 \\
\times \quad \text{101}_2 \\
\hline
\end{array} \]

\[ = 6_{10} \]

\[ = 5_{10} \]

\[ \text{0000} \]

\[ + \quad 110 \]

\[ \text{11110} = 30_{10} \checkmark \]

---

Subtractor

- **Unsigned format**  \( x = 1 - 2 \)

- \( A - B = A + (-B) \)

\[ = A + \overline{B} + 1 \]
\[ \text{carry-in} = 1 \]

\[ \overline{\text{add}} / \text{sub} \]

\[ 0 = \text{add} \]

\[ 1 = \text{sub} \]