One-hot Moore

- 9 states → 5 FFs

<table>
<thead>
<tr>
<th>( Q_4 \ Q_3 \ Q_2 \ Q_1 \ Q_0 )</th>
<th>( \text{N.S.} )</th>
<th>( \text{P.S.} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( S_0 )</td>
<td>0 0 0 0 1</td>
<td>000 0 0</td>
</tr>
<tr>
<td>( S_1 )</td>
<td>0 0 0 1 0</td>
<td>00 1 0 0</td>
</tr>
<tr>
<td>( S_2 )</td>
<td>0 0 1 0 0</td>
<td>01 0 0 0</td>
</tr>
<tr>
<td>( S_3 )</td>
<td>0 1 0 0 0</td>
<td>10 0 0 0</td>
</tr>
<tr>
<td>( S_4 )</td>
<td>1 0 0 0 0</td>
<td>00 0 0 0</td>
</tr>
<tr>
<td>( X = 0 )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( X = 1 )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

N.S. logic: 6 inputs! 64-boot X-map!
N.S. logic

- When does $Q_0^+$ need to be "1"? $S_4$ AND $X=0$.

- When in $S_4$: $Q_4 \cdot \overline{Q}_3 \cdot \overline{Q}_2 \cdot \overline{Q}_1 \cdot \overline{Q}_0$

$Q_4$

$Q_0^+ = Q_4 \cdot \overline{X}$

$Q_1^+ = Q_0 \cdot \overline{X}$

$Q_2^+ = Q_1 \cdot \overline{X}$

$Q_3^+ = Q_2 \cdot \overline{X} + X$

Compare Moore + Mealy

clock

reset

$X$

Moore out: $X_0 X_1 X_2 X_3 X_4 X_5 X_6 X_7 X_8 X_9$

Mealy out: $X_0 X_1 X_2 X_3 X_4 X_5 X_6 X_7 X_8 X_9$
Logic depth - longest path between registers

~50 gate delays: Long
~15-20: Fast
~10: Special processor designs
Guidelines for Efficient State Assignments

Idea: Use binary to assign states

Often assign reset state to 000

One note: use preset also

Guideline I.

Different P.S.
Same input → Same next state

Guideline II.

Different N.B. of one P.S.
Guideline III.

Different P.S.
Same output for all input
Combination

- No min soln guarantee
- Work best w/ D, JK

Guidelines for guidelines

- I. + II. 2 or more lines → high priority
- 3 or 4 states → group of 4 or K-map
- III lower priority
- I preference over II
- Favor N.S. vs. output depending on complexity
16.5] Sequence dat. Mealy

\[ X = 0101101 \]
\[ Z = 0001011 \]

\[ Z = 1 \text{ i.f. } X = \ldots 0110 \]
\[ X = \ldots 101 \]

Q: What needs to be remembered?