UNIVERSITY OF CALIFORNIA, DAVIS
Department of Electrical and Computer Engineering

EEC 18 **DIGITAL SYSTEMS I** **Fall 2024**

LAB 5: COUNTER DESIGN

Objective: Design and build a counter using flip-flops, gates, and a specified counting sequence. Derive the flip-flop input equations using a state table and K-maps

Preparation (Pre-lab)

- Do the *complete* paper design for the counter specified in Design I. Your paper design must include the following:
  - State transition table for the counter
  - K-maps for each of the flip-flop input equations.
  - Minimized sum of products (SoP) equation for each flip-flop input signal.

Description

In this lab, a *unique* counter that follows the state diagram shown in the figure below will be designed. The individualized count sequence is at the end of this document. The count values $X_1 – X_6$ shown in the figure are some sequence of the numbers 1 – 6, with each number used only once. This circuit will simulate rolling a six-sided die.

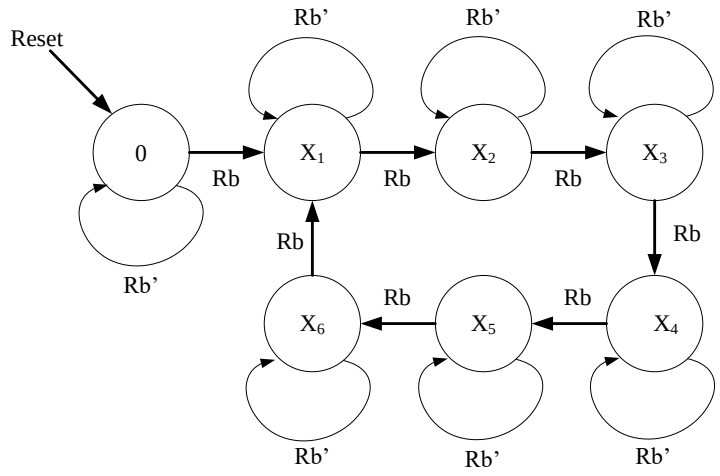

Figure 1. Counter State Diagram

The counter has an input Rb, which stands for “Roll button”. The counter counts as long as Rb = 1, but when Rb = 0, the counter holds the current count value.

There is one other possible state in a 3-bit counter design not shown in Fig. 1. For example, if X_1 to X_6 correspond to a random order of state bits 001 to 110, the unused state has state bits 111 (the reset state is 000). It is possible that the state machine could power-up in this state. Therefore, the state machine should guarantee that it will not remain stuck in this state, even when the reset switch is not pressed. Thus, the next state after the unused state must be to one of the states in the count sequence, X_1 to X_6, or the reset state—it is your choice.

Design I. Moore Machine with the State Bits as the Outputs

Design the counter as a Moore machine where the state bits serve as the counter’s outputs.

a) Draw a state transition table and derive the input equations for implementing the counter using D flip-flops and logic gates.

b) Enter the design in Quartus. Use the 7474 or the DFF component for the D flip-flops, the 7447 component for the seven-segment display logic, INPUT and OUTPUT components and basic logic gates (AND, OR, NOT, etc.) Use

pushbutton switches for Rb and for Reset. Display the output on HEX0. This circuit should be clocked by the 50 MHz clock signal, MAX10_CLK1_50.

c) Verify your design by simulating in ModelSim. Print a copy of the simulation waveforms for one complete cycle for the lab report. Set the radix to hex for the seven-segment output signal. Have your TA verify the simulation.

Simulate with a clock period of 20 ns and run the simulation for 100 ns each step.

Implementation of Design I

Once the simulation for Design I works, download the design to the DE10-Lite board and verify that the circuit works. **Don't forget to import the pin assignments!!** The output will change too fast to observe the sequence while the counter is counting, but it should be observed that the counter stops on numbers 1 to 6 with about equal probability. If the die seems to be "unfair" or certain numbers never appear, check the simulation and the circuit carefully. Another debugging technique is to test the circuit with a slow clock or to replace the 50 MHz clock with a controllable input so the count sequence can be directly observed. Have the TA verify the working circuit.

Design II. Mealy Machine

Design the counter as a Mealy machine. Do a complete *paper* design. However, this design does not need to be implemented as a Quartus schematic or simulated. Compare the number of gates required for the Mealy machine with the number required for the Moore machine in Design I and submit your design and work with your lab report.

Lab Report

Use the format specified in the "Lab Report Requirements" document available on the class web page. Include the following items in your lab report:

- Your **Name**, **Section**, and **Lab Number** with TA verification for circuit simulation and performance
- Graded pre-lab
- Logic design documentation (truth table, K maps, logic equations) for both designs
- Quartus schematics for Design I
- ModelSim simulation waveforms for Design I

Answer the following questions in your Lab Report:

Q1: Compare Design I and Design II of the sequential circuit. Describe any advantages or disadvantages of the Moore design for this circuit.

Q2: A third design for the counter circuit might use a Moore machine where the state bits were not used as the outputs. For example, the state bits might be the binary count sequence 0 – 6. How would this design compare with Designs I and II (assuming your assigned count was not the straight binary count sequence 1 to 6)? Which design is likely to require the fewest gates? Justify your answer.

Grading

▪ Prelab	25 points
▪ Lab Verification (Design I - Simulation)	20 points
▪ Lab Verification (Design I - Hardware)	20 points
▪ Lab Report	35 points
• Mealy machine paper design (Design II)	10 points
• Question Q1	5 points
• Question Q2	5 points
• Quartus schematic	5 points
• Quartus simulation waveform for your unique count sequence	10 points

Last 5 digits of user ID	X1	X2	X3	X4	X5	X6
61402	2	4	6	5	1	3
53250	5	2	6	4	3	1
43732	4	3	6	2	5	1
53015	4	2	6	1	5	3
93870	5	1	6	4	3	2
71050	4	2	6	1	3	5
81555	4	5	6	1	2	3
61788	4	1	6	3	5	2
86442	1	4	6	2	5	3
28230	3	4	6	5	2	1
07105	3	4	6	5	1	2
62660	4	5	6	3	2	1
88765	3	2	6	4	5	1
17399	1	4	6	5	2	3
36270	4	3	6	1	5	2
83416	4	1	6	2	5	3
42280	5	4	6	2	1	3
37900	4	5	6	2	3	1
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19605	1	2	6	3	5	4
85215	5	2	6	1	3	4
28769	5	3	6	4	1	2
69214	5	3	6	2	1	4
36859	4	1	6	3	2	5
47974	1	3	6	5	2	4
00924	5	3	6	2	4	1
31389	4	2	6	5	3	1
34488	5	2	6	4	1	3
54599	5	4	6	1	3	2
57647	1	2	6	4	5	3
75540	1	2	6	5	4	3
14020	2	1	6	5	3	4
05910	5	4	6	2	3	1
30200	4	5	6	3	1	2
99022	1	3	6	4	5	2
80116	2	4	6	1	5	3
22786	4	3	6	1	2	5
22814	1	3	6	2	5	4
72029	3	1	6	5	4	2
78360	1	4	6	5	3	2
36018	4	1	6	5	3	2
95000	1	2	6	5	3	4
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71444	5	4	6	3	2	1
86600	5	1	6	2	4	3
60089	5	1	6	2	3	4
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61430	4	5	6	1	3	2
70464	2	3	6	4	5	1
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07691	4	1	6	5	2	3
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50777	5	1	6	4	2	3
31450	4	5	6	2	1	3
63887	1	4	6	3	5	2
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66758	2	4	6	3	5	1
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