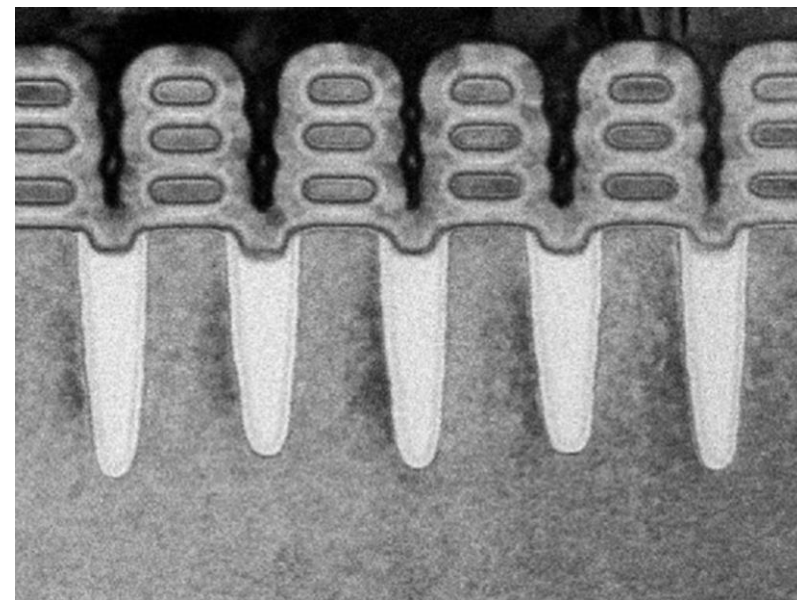
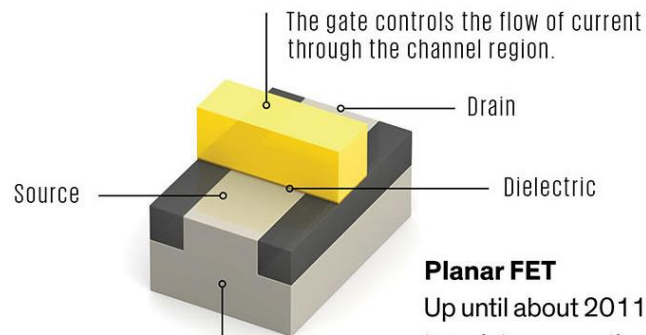


Nanosheet devices are scheduled for the 3-nanometer node as soon as 2021

Only Intel, Samsung, and Taiwan Semiconductor Manufacturing Co. (TSMC) are equipped to operate at this frontier of miniaturization. They are all manufacturing integrated circuits at the equivalent of what is called the 7-nanometer node. Right now, 7 nm is the cutting edge, but Samsung and TSMC announced in April that they were beginning the move to the next node, 5 nm. Samsung had some additional news: It has decided that the kind of transistor the industry had been using for nearly a decade has run its course. For the following node, 3 nm, which should begin limited manufacture around 2020, it is working on a completely new design. That transistor design goes by a variety of names—gate-all-around, multibridge channel, nanobeam—but in research circles we've been calling it the **nanosheet**.

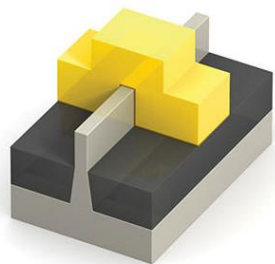


Nanosheet devices are scheduled for the 3-nanometer node as soon as 2021

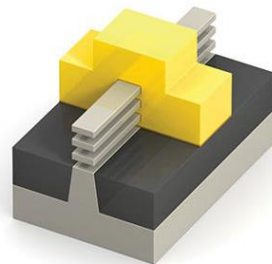


Planar FET
Up until about 2011, planar transistors were the best devices available.

Charge can leak through the channel region and waste power.

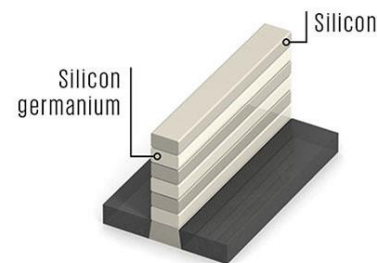


FinFET
Surrounding the channel region on three sides with the gate gives better control and prevents current leakage.

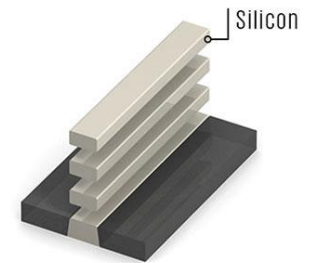


Stacked nanosheet FET
The gate completely surrounds the channel regions to give even better control than the FinFET.

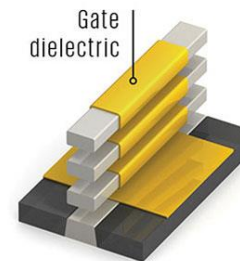
Illustration: Emily Cooper



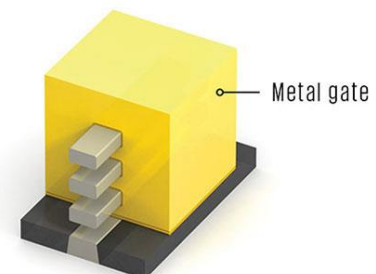
A superlattice of silicon and silicon germanium are grown atop the silicon substrate.



A chemical that etches away silicon germanium reveals the silicon channel regions.



Atomic layer deposition builds a thin layer of dielectric on the silicon channels, including on the underside.



Atomic layer deposition builds the metal gate so that it completely surrounds the channel regions.