Hurdles loom as foundry early adopters sprint toward 45 nm

- The starting gun sounded on the 45-nanometer foundry race last week as the world's largest foundry service provider announced an accelerated ramp for its 45-nm process. But there are signs that the 45-nm node could prove a painful and costly transition for foundry customers.
- Taiwan Semiconductor Manufacturing Co. (TSMC) had planned to release its first "commercial" 45-nm wafers in the fourth quarter but now is shooting for September. Its first 45-nm process is a low-power technology. Volume production is slated for the first half of 2008.
- The foundry giant's main rivals at 45 nm--UMC and IBM Corp.'s technology alliance--are not far behind and plan to ship their respective processes by year's end. IBM's foundry alliance partners are Chartered Semiconductor (Singapore) and Samsung (South Korea).
- It's unclear when--or if--other foundries will enter the 45-nm race, though Fujitsu, Toshiba, China's Semiconductor Manufacturing International Corp. (SMIC) and a few others are expected to field 45-nm foundry processes.

Source: EE Times, "Top Story", April 9, 2007, "Hurdles loom as foundry early adopters sprint toward 45 nm"

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- For now, the question is whether the leading-edge foundries can deliver 45-nm processes without hiccups. The shift from 90 to 65 nm went fairly smoothly, but some fear the 45-nm transition will reconjure the nightmares of the 130-nm node.
- At 130 nm, chip makers introduced a slew of new technologies--such as copper interconnects and low-k--into the process flow. Foundries struggled to deliver chips on time.
- Similarly, the 45-nm node represents the first time that leading-edge foundries will use 193-nm immersion lithography and ultralow-k dielectrics. Foundries are not expected to deploy high-k dielectrics or metal gates in the early stages of the node, however. High-k is still considered unproven for high-volume production.

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- Another question is how quickly foundry customers will embrace 45 nm. IC design costs alone will range between $20 million and $50 million. As for photomask costs, a "mask set" requires an outlay of $500,000 to $800,000 at the 90-nm node and $1.5 million at the 65-nm mode. At 45 nm, photomask costs will be double the 65-nm tally, said Naveed Sherwani, president and chief executive of Open-Silicon Inc.
- That won't deter all customers, Sherwani said, adding that he expects the 45-nm node to be "driven by high-volume chip makers like Xilinx, Intel and TI."
- But many others won't jump on the bandwagon just yet, said Jack Browne, vice president of marketing at MIPS Technologies Inc. (Mountain View, Calif.). Trailing-edge processes "are cheap," Browne said. "These processes will last a lot longer. There are a lot of small guys out there [for whom] $1 million is too much for a mask."

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