2) Electrostatic discharge (ESD)

\[ Q = C \cdot V \]

- \( C \) on chip - small
- modest amount of \( Q \)
- \( V = \frac{Q}{C} \) can go very high!
- destroy gate oxide

ESD diodes

- if \( V_{PAD} > V_{DD} + 0.7V \)
- if \( V_{PAD} \leq -0.7V \)

ESD comes in a brief burst, so an RC helps reduce effect
**SCR - Silicon-controlled rectifier**

![SCR Diagram](image)

4) "Bypass caps" or "Decoupling caps"

- Reduce fluctuations in Vdd/Gnd

![Bypass Capacitor Circuit](image)

Most effective cap: nearest circuit.

But smallest space... """"

→ Smallest cap.

→ Watch out for leakage.
1. On-Chip Transistors
   a) Stel.
      \[ \text{not min. length} \]
   b) Thicker oxide transistor
      - used for I/O circuits
      - lower cap area
      - lower gate current leakage

2. MIM Caps - Metal-Insulator-Metal cups
3) Trench caps
   - found in processes that support DRAM

5) High current wires other than VDD/ground

Ex. clock tree
   → RC delay
   → electromigration

6) Electromigration
   - Wear-out failure for high current
     low cross-sectional area metal wire
   - metal atoms move

   I →
   - worse for DC
   - worse at high temps
7) High current distributed loads

1) Chain of inverters - lumped C

2) Distributed C

3) Clock tree
   - FFs distributed
   - low clock skew
H-Tree
- distrib. C
- low skew

(one clic network node)

(source (as example))
FIB units of circuits

Spare Gates

Packages
  • Rents Rule
  • Solder
    • System - PWB - Pkg - Chip
  • Chip to Pkg
    1) Wire bond
    2) TAB
    3) Flip chip solder bump
  • Pkg-to-Board
    1) Through hole
    2) SMT
      a) Bump-wings
      b) J-lead
      c) solder balls

Packages!
  • Multi-chip modules
  • 3D: TSVs, stacked die

Ann
  • tileable, about