Top: drains

1. Top level metal
   600 x 600 μm - 1500 μm x 1500 μm
   - often all metal layers
   - via on side of pad
   - no circuits below pad

2. Opening in passivation
   53 μm

3. Pitch
   80 - 150 μm
   80 μm
2) Opening in glass

**Types of pads**

- Power (Vdd, Gnd)
- Input
- Output
- I/O

![Diagram of pad types](image-url)
- Corner pads

**Output drivers**

- Massive
- Folded
- Separate NMOS & PMOS more
- Surround MOS of PWC or NWC
  - "Guard ring" - for latchup

[Diagram of output drivers]
2) Electrostatic Discharge (ESD)

\[ Q = CV \]

chip: \( C \) is very small

moderately \( Q \rightarrow V \uparrow \) high

- ESD diodes

- Low-pass filter

- Silicon-controlled rectifier (SCR)
3) Power/Gnd Grids
   a) Vdd/Gnd "Power Rings"

   b) Vdd/Gnd grid over chip
      - where it makes sense
      - top level metal 2x thicker

4) Bypass or Decoupling Capacitors
   Reduce fluctuation in Vdd/Gnd
   cheaper ➔ more effective
On-Chip Caps

a) std MOS

- NOT min. length
- leakage

b) Use 2nd type MOS, thicker gate oxide

c) Metal-Insulator-Metal (MIM) caps

m∠: 60°
m∠: 90°

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5) High-Current Wires

- Use wider metal

Ex: clock

![OC circuit](image)
6) Electromigration
   - only in metal

   I →

   a) E field
   b) momentum of ions

   - worse for DC than AC
   - worse at high temps

7) High-voltage-driven leads

   1) Clean or rinse
   2) Dist. rinse
   3) "H tree"
Office

Hour

10 cm \times 1 \text{mm} = (10^5 \text{mm} \times 1 \text{mm}) \times 3 \text{mm}^2 = 3 \text{pF}

10 \text{cm} \times 2 \times 40 \text{pF/mm}

\frac{1}{C_0}

\frac{1}{C'}