Dimentions:

1) Pad size: $60\mu m \times 60\mu m - 100\mu m \times 100\mu m$

2) Glass opening: $70\mu m \times 50\mu m - 90\mu m \times 90\mu m$

3) Pad pitch: $80\mu m - 150\mu m$

- Power
  - via, bond
- Input
- Output
- I/O
- Chip
Output driver

- massive for off chip loads
- folded transistors!
- separate Nmos and Pmos by some distance
- surround with well/substrate (i.e. "guard ring")
3) Power and Ground Grids

Goal: low R, high I from pads to circuits

a) start out "power rings" around circuits just inside pads

b) circling taps power from ring

5) Add Vdd/Gnd grid over entire chip
   - where it makes sense
   - as wide as possible/reasonable

Remember top-level metal is thickest
so favor top-level metal