Modeling a distributed RC wire for simulation

1. Break up into N pieces

\[ \frac{R_{\text{total}}}{N} \]

\[ \frac{C_{\text{total}}}{N} \]

2. "T" models "T"

\[ \frac{R/2}{C} \]

\[ \frac{R/4}{C/2} \]

3. "Π" models "Π"

\[ \frac{R}{C_2} \]

\[ \frac{R}{C_4} \]

\[ \frac{R/2}{C_4} \]

\[ \frac{R/2}{C_4} \]

* Π3 model within 3% of actual distributed RC
Transmission lines

Model w/ trans. lines when time of flight is comparable to t₁ and tₙ.

Signal velocity \( v = \frac{1}{\sqrt{LC}} \)

\( L = \text{inductance/length} \)

\( C = \text{capacitance/length} \)

Characteristic impedance \( Z₀ = \sqrt{LC} \)

Typical \( Z₀ \) on chips = 10Ω - 200Ω

Classic \( Z₀ = 50Ω \)

Nvidia NVLink: 85Ω
1) Parallel Termination

2) Series Termination

3) Thru Ring

4) Ac
Std Cell Place & Route

1) "Front End"
   - Verilog
   - Synthesis $\rightarrow$ gate-level netlist
   - Gate-level simulation

2) "Back End"
   - P&R
   - DRC
   - LVS
   - $\equiv$

Verilog: $c = !a \land b$

![Diagram of Verilog logic](image)

P&R:

![Diagram of P&R logic](image)
Chip-level Structures and Issues

1) Input/Output of chip

- Large metal regions on chip for I/O

a) Standard wire bonds
   - On periphery

b) Double row of pads

c) Area pads

   + Lower R + C
   + Signals
   + Vdd / Gnd
Typ. drains

1) Top level metal
   60 x 60 µm - 100 x 100 µm
   - often all metal layers
   - vias on side of pad
   - no circuits below pad

2) Opening in passivation

3) Pitch
   80 - 150 µm

50 x 50 - 90 x 90 µm