1) Simplest

\[ T_p = 0.69 \cdot R \cdot C \]

2) Split up wire

\[ R_i = \frac{R_{\text{TOTAL}}}{N} \]
\[ C_i = \frac{C_{\text{TOTAL}}}{N} \]

For large \( N \), using Elmore delay eqn,

\[ T_{DN} = \frac{R_i C_T}{2} \]

Let \( L = \) length of wire
\[ R_T = r \cdot L \]
\[ C_T = c \cdot L \]

\[ T_{DN} = \frac{r \cdot c \cdot L^2}{2} \approx \frac{T a L^2}{2} \]
3) Distributed RC line

P.D.E. \( V \), \( \tau C \frac{dV}{dt} = \frac{d^2V}{dx^2} \)

diffusion equation

\[ 0 \rightarrow \frac{V_{DD}}{2} \text{ at end of wire} \]

\[ t_p = 0.38 \frac{R_C}{C} = 0.38 (RL)(RL) = 0.38 vC L^2 \]
<table>
<thead>
<tr>
<th>Input to wire</th>
<th>Output of wire</th>
<th>Lumped RC</th>
<th>Distributed RC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0 → ( \frac{\text{Vdd}}{2} )</td>
<td>0.69 ( R \cdot C )</td>
<td>0.38 ( R \cdot C )</td>
</tr>
<tr>
<td></td>
<td>0 → 63% (( t ))</td>
<td>( R \cdot C )</td>
<td>0.5 ( R \cdot C )</td>
</tr>
<tr>
<td></td>
<td>10% → 90% (( t_r ))</td>
<td>2.2 ( R \cdot C )</td>
<td>0.9 ( R \cdot C )</td>
</tr>
</tbody>
</table>

RC wire delays should be considered when they are a significant fraction of the gate delay.

To reduce wire delays:

1) Make wires shorter - layout
2) Maybe increase wire width
   \( R \downarrow \)
   \( C \uparrow \)

Most helpful on poly
3) Use higher level of metal
   
   Caution: Watch out for intra-layer cap.

4) Pipeline circuit
   
   \[ C = \varepsilon \frac{A}{\ell} \]
   
   \[ 3 \cdot (k \cdot r \cdot c \left( \frac{L}{3} \right)^2) + 2 \cdot \text{Delay of inverters} \]
   
   \[ = (k \cdot r \cdot c \cdot L^2) \cdot \frac{1}{3} + \frac{1}{3} + \frac{1}{3} + \frac{1}{3} + \frac{1}{3} \]

2.5) Increase wire spacing

5) Adding repeaters
1) Break into N small pieces

2) "T" models

3) "π" models

"π3" error < 3%
Transmission Lines

- Signal moves as a wave down wire
  
- Typical on-chip char. impedance $Z_0$
  
  $10 \Omega - 200 \Omega$

  $50 \Omega$ Classic

  $85 \Omega$ Nepomi, Zcc, Nvidia NVLink

1) Parallel Termination

2) Series Form

$$R = Z_0 - Z_d$$

$Z_d =$ driver output impedance

3) Thevenin
1) AC

- ac + DC current

Chip-level Structures and Issues

1) Input/output to/from chip

- Standard wire bonds
  - pads on periphery

- Dense double-row of pads
  - slightly more prone to mistakes
c) Area pads

- Flip chip package
- Many more signals
- Lower R, C
  - Signals
  - Vdd, Gnd

Typical dimensions of pads

- Top metal square
  - 60μm × 60μm
  - 100μm × 100μm
- Often a stack of all metals
- Vias often off to side!
- No circuits below