4:1 Mux

\[ a \quad \overline{s_1} \overline{s_0} \]
\[ b \quad s_1 \overline{s_0} \]
\[ c \quad s_1 s_0 \]
\[ d \quad \overline{s_1} s_0 \]

\[ \text{out} \]

\[ a \quad 00 \]
\[ b \quad 01 \]
\[ c \quad 10 \]
\[ d \quad 11 \]

\[ \text{out} \]

\[ \overline{s_1} \overline{s_0} \]

\[ a \quad \overline{s_1} \overline{s_0} \]
\[ b \quad s_1 \overline{s_0} \]
\[ c \quad s_1 s_0 \]
\[ d \quad \overline{s_1} s_0 \]

\[ \text{out} \]

\[ \text{buffer output} \]

\[ \text{buffer output} \]
b) Transmission Gate Logic

N/MOS $\rightarrow$ trans. gate

\[ a \quad \bar{b} \]
\[ \quad \Rightarrow \quad \]
\[ a \quad \bar{b} \]

\[ V_{dd} \]
may still buffer to increase drive current

Big picture
**Exercise 2.1: 2:1 multiplexer**

![Diagram of a 2:1 multiplexer]

- **Might add inputs**
- **Incorporate area a lot**

<table>
<thead>
<tr>
<th></th>
<th>Only PDN on</th>
<th>Only PDN off</th>
<th>Both PDN on</th>
<th>Neither PDN on</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static</strong></td>
<td>out = 1</td>
<td>out = 0</td>
<td>transition</td>
<td>never</td>
</tr>
<tr>
<td><strong>Dynamic</strong></td>
<td>Precharge</td>
<td>Evaluate</td>
<td>never</td>
<td>Evaluate phase</td>
</tr>
<tr>
<td></td>
<td>phase</td>
<td>phase &amp; out = 0</td>
<td></td>
<td>out = 1</td>
</tr>
<tr>
<td><strong>Ratified</strong></td>
<td>out = 1</td>
<td>never</td>
<td>out = 0</td>
<td>never</td>
</tr>
</tbody>
</table>
Chapter 4 - Wires

Chip consists of (physical view)

1) Transistors for "work"
   - Datapath
   - Memory
   - Control

2) Wires
   - Signals
   - Vdd / Gnd

3) Misc
   - I/O pads

- Signals can be routed using:
  1) diffusion (N or P) only very short distances
  2) poly (for short distances)
  3) metal (common)

- Power / Gnd
  "Always in metal"
Wire capacitance

A) "Bottom plate"

\[ C = \varepsilon \frac{W \cdot L}{t} \]

\[ \varepsilon = \text{permittivity} = \varepsilon_r \varepsilon_0 \]

\[ \varepsilon_0 = 8.854 \times 10^{-12} \text{ F/m} \]

\[ \varepsilon_r = 1 \text{ free space} \]

\[ \varepsilon_r = 3.9 \text{ air} \]

B) Fringing

C) Estimate bottom plate + fringing cap

\[ C_{PP} + C_{image} = \frac{W - H/2}{t} + \frac{2\pi \varepsilon}{\log (2t/H + 1)} \]

PM-dominates
Traditional wires

- wider + flatter wires
- fewer levels
- long tr and tf
  - neglect $L \frac{di}{dt} \sim 0$

- gate delay $\gg$ wire delay
  \[ \therefore \text{ neglect } R \text{ wire} \]

- Trad. wire model
  - $R \text{ wire} = 0$
  - All cap. is to substrate
  - Inductance $\approx 0$

Modern wires

- smaller and thinner
- higher $R$
- intra-layer cap. significant
- fast $t_r$ and $t_f$
  - $L$ important
- old: $5V, 5W \rightarrow 1$ Amp
  
  now: $1.1V, 50W \rightarrow 45$ Amps
  
  - $L$ and $R$ important for vad/and
- levels of metals
  1. $1.0\mu m$ CMOS
  2. $0.18\mu m$
  3. $0.13\mu m$
  4. $0.14\mu m$ IBM POWER 9

\[ \text{Ex: for } 0.25\mu m \text{ CMOS } \Rightarrow \lambda = 0.125\mu m \]