1) NMOS
2) CMOS "pseudo NMOS"

**James:**

- Four input caps.
- Good speed.
- Small area.
- When out = 0, static current (very bad) "short-circuit current".
- Careful design for load.
- Poor logic levels:
  - NMOS: 0, Vdd-Vt
  - Pseudo NMOS: 0

### III. Dynamic

- PMOS & clocked PMOS

Schematic:

- Output signal change:
  - Input: "charge"
  - Pre-charged: 0
  - Evaluate: 1
  - Output: 1
  - Output: 0
+ can eliminate static power
+ in general, the fastest style
+ small area
+ good 0, 1
- clk to all logic gates
- clk power - 200% activity
- if out = 1, out "floats" (hi-z) during evaluate
  - reliability
- can't stop or slow (too much) the clock
  - clock gate
  - testing

III. Pass transistor logic

- inputs also drive source/drain(s)
- inputs provide Vdd/Gnd to output(s)

Ex: AND
Ex: XOR

Ex: XNOR easy

Ex: 2:1 Mux