Ch. 6 - Logic Gates

AND, OR, NOT

XOR

nand, ea

CMOS: NAND, NOR, NOT (INV)

I. Static Circuits

out comm. to Vdd/Gnd thru low resistance

Ex: 2-input NAND

<table>
<thead>
<tr>
<th>a</th>
<th>b</th>
<th>out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>high</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>M1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>M2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>M3 source to M4 to Gnd</td>
</tr>
</tbody>
</table>

Building complex gates:

1) Nmos "on" when input high v
PMOS "off" low v

2) PUN: active when OUT = 1
PDN: "off" = 0
3) PMOS's pull up well
   NMOS's "down"

4) OR: think parallel
    1 → A OR B

    AND: think series
    1 ← A & B

Ex: \( \text{out} = (A+B) \cdot (C+D+E) \)

\( \text{PDN (NMOS)} \): when is \( \text{out low} \)?
   \( (A+B): (C+D+E) \) is high/true/active

\( \text{out} = (A+B) \cdot (C+D+E) \)
**PUN (P Livingston): When is out high?**

\[ \text{out} = \overline{A} \cdot \overline{B} + (C \cdot D \cdot \overline{E}) \]

but we need the equation for out as a function of \( \overline{A}, \overline{B}, \overline{C}, \overline{D}, \overline{E} \)

\[ \text{out} = (A + B) + \overline{(C + D + \overline{E})} \quad \text{[DeMorgan's]} \]

\[ \text{out} = (\overline{A} \cdot \overline{B}) + (C \cdot \overline{D} \cdot \overline{E}) \]

\[ a = 0 \rightarrow \overline{a} \]

\[ a = 1 \rightarrow \overline{a} \]
Delays of gates

1) Gates more complex than inverter

   - Delay depends on inputs

      Ex: 3-input NOR

         * Hi → Low
           one input high

            \[ t_p = 0.69 R_n C_L = t_p_0 \]

         * Two inputs high

            \[ t_p = 0.69 R_n C_L \cdot \frac{1}{2} \]

         * 3 inputs high

            \[ t_p = \frac{1}{3} t_p_0 \]

2) Need to increase widths to balance delay

Assume 2: \[ R_{NMOS} = R_{PMOS} \]

\[ \text{Llew} \]

* NMOS

\[ W = 2 \text{mm} \]

\[ W = 1.5 \text{mm} \]
* 3-input NOR

\[ R_{\text{PUN}} = 3 \cdot R_{\text{PUNOS}} \]

\[ R_{\text{PDN}} = R_{\text{NUNOS}} \text{ worst case} \]

So, to maintain \( t_P = t_P \) in the worst case,

\[ W_{\text{PUNOS}} = 6 \cdot W_{\text{NUNOS}} \text{ inverter} \]

\[
\begin{cases}
  \text{eff.} \quad W_P = 1 \text{ mm} \\
  \text{eff.} \quad W_n = 1 \text{ mm}
\end{cases}
\]

\( \text{total 21 mm "width"} \)

* 3-input NAND

\[
\begin{cases}
  W_P = 2 \text{ mm} \\
  W_n = 3 \text{ mm}
\end{cases}
\]

\( \text{total 15 mm "width"} \)

3) Large fan-in gates

\[ N \text{-input NAND} - N \text{ NUNOS in series} \rightarrow \text{each } \sim N \text{ larger} \]

\[ \text{NOR} - \text{"PMOS"} \rightarrow \ldots \]
Solutions:

a) Increase transition sizes

b) Input reordering
   - place inputs to trans.
   - nearest Gnd/Vdd

c) Taper trans., stack
   - may be inefficient
   - in layout

d) Restructure
   - Ex: 5-input AND

\[ \text{Diagram of circuit components} \]
II. Ratieed

Before CMOS, NMOS

NMOS load must be:

1) weak enough - PDN can overpower it

2) strong enough - reasonable tr