Chapter 6: Comb. Logic Gates

I. Static Circuits

Example: 2-input NAND

<table>
<thead>
<tr>
<th>a</th>
<th>b</th>
<th>out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>m1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>m2 to Vdd</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>m1 to Vdd</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>out low</td>
</tr>
</tbody>
</table>

General static gate circuit

1) NMOS "on" when its gate is high
   PMOS "off" low

2) PUN: active when OUT=1
   PDN: "off" OUT=0

3) PMOS' pull up well, pull down poorly
   NMOS' pull up poorly, pull down well
4) OR function: picture parallel

AND function: picture series

Ex: \( \text{out} = (A+B) \cdot (C+D+E) \)

PDN (NMOS)

Q: When is \( \text{out} \) low?

When \( (A+B) \cdot (C+D+E) \) is true (high)

\( \text{out} = (A+B) \cdot (C+D+E) \)
PUN (PMOS)

When is out high?

\[ \text{out} = (A+B) \cdot (C+D+E) \]

But for PMOS, they need their gates low to be active

\[ \implies \text{Anchir of } \overline{A}, \overline{B}, \ldots \]

\[ \text{out} = (A+B) + (C+D+E) \quad \text{[DeMorgan's]} \]

\[ \text{out} = (\overline{A} \cdot \overline{B}) + (C \cdot D \cdot E) \quad \text{[.. =]} \]

Active when \( \overline{A} = 1 \)
\[ A = 0 \]

\[ \text{-- Book method} \]
Delays at cells

1) More complex than an inverter
   a) Delay depends on data - input values

   Ex: 3-input NOR
   out hi → low
   1 input high:

   \[ R_{N} = C_{L} \]

   2 inputs high: ab, ac, bc
   \[ R_{pull-down} = R_N / 2 \]

   3 inputs high: abc
   \[ R_{pull-down} = R_N / 3 \]

2) "Need" to widen series transistors to balance delays
   Assume \( R_{PMOS} = 2 R_{NMOS} \) for equal \( W, L \)

Inverter

\[ W = 2 \mu m \]
\[ L = 1 \mu m \]
Ex: 3-input NOR

\[ R_{PD\text{N}} = 3 \cdot R_{P\text{MOS}} \]

\[ R_{PD\text{N}} = R_{N\text{MOS}} \text{ in the worst case} \]

So for balanced delays that match the inverter,

\[ W_{PMOS} = 3 \cdot 2 = 6W_{NMOS} \]

\[ \text{Total widths} = 21\mu m \]

Ex: 3-input NAND

\[ \text{Total widths} = 15\mu m \]

NAND preferable to NOR in general
3) Large Fan-in Gates

N-input NANO: N NMOS in series $\rightarrow$ each $\sim N \times$ larger

N-input NOR: N PMOS

Delay will increase for each input

Area $\ldots \ldots \ldots$

Solutions

a) Keep incr. transistor sizes

b) Input reordering
- earliest input to transistor
- nearest VDD or GND
- early signal change/discharge

Internal caps $\rightarrow$ earliest input

CLK $\rightarrow$ a

b $\rightarrow$ c $\rightarrow$ d $\rightarrow$ e
c) Taper transistor stack
   - progressive sizing

   - doesn't layout as well often

   earliest input

   virtual ground

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d) Restructure

Ex: 5-input AND

Diagram of 5-input AND gates
II. Ratioc

Before CMOS, there was NMOS (only)

NMOS load device

- strong enough for reasonable rise time
- weak enough that the PDN can overpower it