A) Inverter capacitance

1) gate-to-drain overlap
   - Miller capacitance

2) gate-to-source
   - does not affect driving of inverter a

3) drain to bulk

4) source to bulk - good cap. on end node

5) wire capacitance

6) load capacitance
   a) other gates
   b) other source/drain diffusions

B) Inverter driving resistance

\[ \text{Req} = \text{equiv. resistance} \]
\[ \text{Req}_W = 13 \, \text{k}\Omega \text{ when } W = L, \ 0.25 \, \text{um CMOS}, \ V = 2.5 \text{V} \]
\[ \text{Req}_L = 31 \, \text{k}\Omega \]

\[ \text{Req} = \frac{\text{Req}_W}{\left( \frac{W}{L} \right)} \]
Increasing Performance

1) Reduce load capacitance.
   - Layout
     - shorter lines
     - smaller loads
   - Algorithm
     Ex: $A'B + A'B' = A'$

2) Reduce Reg (increase drive current)
   - Decrease $\frac{W}{L}$ → wider transistors
   - Increase $Vdd$ — maybe not possible
     - Max $Vdd$
     - Power budget

Diagram:

- Vertical axis labeled $t_p$
- Horizontal axis labeled $Vdd$
- Plot points and lines
- $t_p = 0.59$ Reg $C_L$
3) Adjust PMOS/NMOS ratio

\[
\beta = \frac{W/L_{PMOS}}{W/L_{NMOS}}
\]

\[
\beta = \frac{W_{PMOS}}{W_{NMOS}} \quad \text{with} \quad L_N = L_P
\]

If we neglect wire capacitance (large, close inverters)

Two identical inverters:

\[
\beta_{opt} = \sqrt{\frac{R_{eqP}}{R_{eqN}}} \quad \text{for lowest} \quad t_P \quad \text{p. 204}
\]

\[
t_P \quad 50\,\text{ps} \quad t_{PLH} \quad t_{PHL} \quad t_P
\]

\[
40\,\text{ps} \quad 154 \quad 1.9
\]

\[
30\,\text{ps} \quad 1 \quad 2 \quad 2.4 \quad 3 \quad 4 \quad 5 \quad \beta
\]
For $0.25 \mu m$, $2.5V$

- For $t_{\text{PHL}} = t_{\text{PLH}}$

$$
\beta = \frac{\text{Req} \ p}{\text{Req} \ n} = \frac{31 \ \text{kQ}}{13 \ \text{kQ}} = 2.4
$$

- For min. delay,

$$
\beta_{\text{opt}} = \left[ \frac{\text{Req} \ p}{\text{Req} \ n} \right]^{1/2} = 1.54 - \text{theory}
$$

- From circuit simulation

\[ \beta_{\text{opt}} \approx 1.9 \]

"Chain of inverter's problem"

First, some background:

- $C_g =$ input gate cap.
- $C_{\text{int}} =$ intrinsic output cap. (mostly diff. cap.)
- $C_{\text{ext}} =$ external cap. to inv. (wire + $C_L$)

Ex: - clock network
- I/O ports

\[ \text{Huge } C_L \]
\[ \text{fint} = \frac{\delta \cdot C_g}{\gamma} \]

\[ \gamma = 1 \text{ for modern processes} \]

\[ f = \text{effective fanout} = \frac{C_{\text{ext}}}{C_g} \]

\[ t_p = t_{p_0} + t_{i_0} \frac{f}{\gamma} \]

- function of \( f \) only! Key point

\[ \frac{f}{\gamma} = \frac{C_{\text{ext}}/C_g}{C_{\text{int}}/C_g} \]

\[ \frac{f}{\gamma} = \frac{C_{\text{ext}}}{C_{\text{int}}} \]

```
 1 f f^2
```

N = number of stages

\[ F = \text{overall effective fanout} = \frac{C_L}{C_{g_1}} \]

\[ C_{g_1} = C_g \text{ of first inverter} \]

\[ f = \sqrt[N]{F} \]

Choose \( N \) to minimize delay for a given \( F \)
1) Assume $y = 0$ - a Circuit simplification

$$N = \ln (F)$$

\[ f = e^{-2.718} \]

2) $y = 1$ - realistic

Cannot solve in closed form

Solve numerically

\[ f \approx 3.6 \]

- Too low $f$ is very slow
- Lower $f$ → more gates

Ex: $F = 50$, neglect inversions (odd or even $N$ are ok)

First inv. $W_1 = 6\lambda$, $W_2 = 4\lambda$

- $N = 2$: $f = \frac{2}{\sqrt{50}} \approx 7$
- $N = 3$: $f = \frac{3}{\sqrt{50}} \approx 3.8$ (✓)
- $N = 4$: $f = \frac{4}{\sqrt{50}} \approx 2.8$
If oversims are not allowed, then we must choose an odd or even N, or...

a) Use a output

b) DFF input
c) absorb into logic

\[ \text{Diagram showing logic gates and variables.} \]