Momories

1) Latches

2) FFS

- setup time
- hold time
- clk-to-Q

Timing Requirements

1) Comb. logic is not too slow

\[ \text{clk cycle time} \geq t_{\text{clk-to-Q}} + t_{\text{logic max}} + t_{\text{setup}} \]

2) Comb. logic is not too fast

\[
\left( t_{\text{clk-to-Q min}} + t_{\text{logic min}} - t_{\text{clk skew}} \right) \geq t_{\text{hold}}
\]

- a) 2 cycle Skip through
- b) violate hold time

\[ \rightarrow \text{Fail!} \]
8 gates driven by clk + \overline{clk}

Local clk buffering

+ 1 clock input into FF
+ min clock skew

"safest" FF

clock

smaller

longer
Ch.5 - CMOS Inverter

- **Vin** is "high"
  \[ V_{in} > V_{dd} - V_{TP} \]

- **Vin** is "low"
  \[ V_{in} < V_{TN} \]

3. \[ V_{dd} - V_{TP} \geq V_{in} \geq V_{TN} \]
   - Both NMOS and PMOS on
   - Brief transient state
   - Ignore for simple analysis
\[ V = \frac{K_p V_{sat-p}}{K_n V_{sat-n}} \]

\[ = \frac{V_{sat-p} W_p}{V_{sat-n} W_n} \]

\[ V_M = \frac{r \cdot V_{dd}}{1 + r} \]

Find balanced case of \( V_M = \frac{V_{dd}}{2} \)

\[ \frac{V_{dd}}{2} = \frac{r \cdot V_{dd}}{1 + r} \quad \Rightarrow \quad r = 1 \]

\[ l = \frac{V_{sat-p} \cdot W_p}{V_{sat-n} \cdot W_n} \]

\[ \frac{W_p}{W_n} = \frac{V_{sat-n}}{V_{sat-p}} \]

P. 186

0.25 mm CMOS

2.5 V VDD

Adjust \( V_M \) to

a) maximize noise margins
b) interface \( V_M \) with an unbalanced signal.
Ex: TTL 5V

TTL

2.4

0.4

V_m

Ideally \( V_m = \frac{2.4 + 0.4}{2} = 1.4 \text{ V} \)

C1 Higher performance

PMOS: \( \sim 2 = 3.5 \times \text{ lower current per size } \) compared to NMOS

\( \rightarrow \) Use smaller PMOS

\( l = 2.7 \)

\( W = 39 \ \Omega \)

\( W = 10 \ \Omega \)

\( W = 34 \ \Omega \)

\( W = 10 \ \Omega \)

\( W = 20 \ \Omega \)

\( W = 10 \ \Omega \)

Pull down much faster

Pull up slower or slightly slower.
For 2 stages

<table>
<thead>
<tr>
<th></th>
<th>1st Inv</th>
<th>2nd Inv</th>
</tr>
</thead>
<tbody>
<tr>
<td>x ↑</td>
<td>slower</td>
<td>much faster</td>
</tr>
<tr>
<td>x ↓</td>
<td>much faster</td>
<td>slower</td>
</tr>
</tbody>
</table>

- Net speedup

- Reduced noise margins

- Area smaller

- Lower total $C_L$ $\Rightarrow$ lower energy + power