Memory

I. Single-bit

A) Clockless latches

B) Transparent latches

C) Fees

II. Array

Transparent latches

Diagram:

- Transp. high latch

No fighting
2) Flip-Flops - Master-Slave FF

- Setup time
- Hold time
- clk-to-Q delay
1) Comb. logic can not be too slow

\[ \text{clk cycle time} \geq t_{\text{clk-to-q}} + t_{\text{logic max}} + t_{\text{setup}} \]

Assumes clock skew = 0

2) Comb. logic not too fast (slower than ~clock skew)

\[ t_{\text{clk-to-q}} + t_{\text{logic min}} - t_{\text{clk-skew}} \geq t_{\text{hold}} \]

"Hold time violations"

Flip-Flop

See handout for schematic

Buffer clk inside each FF
CMOS Inverter

1. $V_{in}$ "high"
   - $V_{in} > V_{dd} - V_{tp}$

2. $V_{in}$ "low"
   - $V_{in} < V_{tn}$

3. Both NMOS and PMOS on
   - brief transient region
   - ignore for simple analysis

Switching threshold $V_{th}$

![Diagram of CMOS Inverter](image)
Assume devices are velocity saturated

\[ r = \frac{k_p \cdot V_{sat p}}{k_n \cdot V_{sat N}} \]

\[ = \frac{V_{sat p} \cdot W_p}{V_{sat n} \cdot W_n} \]

\[ V_m = \frac{r \cdot V_{dd}}{1 + r} \]

Find balanced point: \( V_m = \frac{V_{dd}}{2} \)

\[ \frac{V_{dd}}{2} = \frac{r \cdot V_{dd}}{1 + r} \]

\( r = 1 \)

\[ 1 = \frac{V_{sat p} \cdot W_p}{V_{sat n} \cdot W_n} \]

\[ W_p = \frac{V_{sat n}}{V_{sat p}} \]

\[ W_n = \frac{V_{sat p}}{V_{sat n}} \]

\( p = 1.86 \)

\( 0.25 \text{ mm}, 1.25 \text{ mm} \)

\( 1.5 \text{ V}, 1.25 \text{ V}, 1.0 \text{ V} \)

\[ W_p/W_n \]
Adjust $V_m$ to:

a) Max. noise margins

b) Interfacing with unbalanced signals

Ex: TTL 5V

Max. noise margin $V_m = 1.4V$

c) Higher performance

PMOS $\sim 2-3.5$ less current per "size"

- Use smaller PMOS

\begin{align*}
\text{balanced} \quad \text{W}=34 \\
\text{W}=10
\end{align*}

\begin{align*}
\text{faster} \quad \text{W}=20 \\
\text{W}=10
\end{align*}
- Pull down much faster
  - Pull up slower, or slightly slower
  - Faster for 2 stages

<table>
<thead>
<tr>
<th>1st Inv</th>
<th>2nd Inv</th>
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</thead>
<tbody>
<tr>
<td>Fall</td>
<td>Much faster</td>
</tr>
<tr>
<td>Rise</td>
<td>Slower</td>
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</tbody>
</table>

- Smaller noise margins
- Smaller area
- Lower total $C_L \rightarrow$ lower energy

A) Intrinsic Capacitances

1. Gate-to-drain overlap, Miller
2. Gate-to-source
does not affect part of driving inverter
3. Drain to bulk
4. Source to bulk, good, smoother Vdd/6vdd
5. Wire
6. Load, etc. Normally gate cap.