Contact / Via resistance

Typical 0.15 μm

N+ - M1 11 Ω
P+ - M1 11 Ω
Poly - M1 10 Ω
M1 - M2 5 Ω

\[
\begin{align*}
\text{In mask:} & \\
\text{P+ - M1} & 11 \Omega \\
\text{M1 - Pmos} & \frac{11}{3} \Omega
\end{align*}
\]

Scaling

s scaling factor

Tech1 → Tech2, \( s = \frac{\text{Tech1}}{\text{Tech2}} \)

Ex: 65nm → 32nm \( s \approx 2 \)

V scaling factor for voltages
K for $s$

Ni3 proposed scaling:
1) Dimension $K$ "vertical" and "horizontal"

2) Voltage $V_{ds}$

3) Doping

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Relation</th>
<th>&quot;Full Scaling&quot;</th>
<th>General</th>
<th>(U = 1) Fixed-Voltage Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W, L, t_{ox}$</td>
<td>$1/s$</td>
<td>$1/s$</td>
<td>$1/s$</td>
<td>$1/s$</td>
</tr>
<tr>
<td>$V_{dd}, V_T$</td>
<td>$1/s$</td>
<td>$1/s$</td>
<td>$1/u$</td>
<td>$1$</td>
</tr>
<tr>
<td>Area/Device</td>
<td>$1/s^2$</td>
<td>$1/s^2$</td>
<td>$1$</td>
<td>$1$</td>
</tr>
<tr>
<td>$C_{ox}$</td>
<td>$1/t_{ox}$</td>
<td>$1$</td>
<td>$1$</td>
<td>$1$</td>
</tr>
<tr>
<td>$C_{gate}$</td>
<td>$C_{ox} \cdot W \cdot L$</td>
<td>$1/s$</td>
<td>$1/s$</td>
<td>$1$</td>
</tr>
<tr>
<td>$R_{on}$</td>
<td>$1$</td>
<td>$1$</td>
<td>$1$</td>
<td>$1$</td>
</tr>
<tr>
<td>Intrinsic delay</td>
<td>$R_{on} \cdot C_{gate}$</td>
<td>$1/s$</td>
<td>$1/s$</td>
<td>$1$</td>
</tr>
<tr>
<td>Power</td>
<td>$I_{sat} \cdot V$</td>
<td>$1/s^2$</td>
<td>$1/s^2$</td>
<td>$1/s^2$</td>
</tr>
</tbody>
</table>

![Circuit Diagram](image)
Chapter 7 - Sequential Circuits

Real System

Clock signal - pace the flow of data in a digital system
I. Single-bit

A) Clockless latches
   e.g. SR latch

B) Transparent latches

C) Edge-triggered Flip-Flops

II. Array

- address
- array of cells

Clock Networks

- signal routed to all memory elements (very high demand)
- also likely highest capacitance signals on chip
If clock has \( f = 1 \text{ GHz} \),

\[ \frac{1}{f} = \text{clock period} = \frac{1}{16 \text{ GHz}} = \frac{1}{10^9 \text{ Hz}} = 10^{-9} \text{ sec} \]

\[ = 1 \text{ nsec} \]

\[ \therefore \text{ all logic paths must take less than 1 ns} \]

Clock system:

Clock gate turns off clock for a portion of the chip
- logically equivalent to AND
- enable signal

Oscillator

odd # of invs in the ring
Phase-Locked Loop (PLL)
- analog circuit
- locks to a reference frequency
- contains a tunable ring oscillator

Delay-Locked Loop (DLL)

1) Transparent latch
   a) Dynamic
      - when clk = 0, node x "floats"
      - very small

   b) Static
      - Fight!

<table>
<thead>
<tr>
<th>Old Value</th>
<th>New Value</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>no work!</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>tough up</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>ok</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>no work!</td>
</tr>
</tbody>
</table>