- All V_{out}
  \[ \text{Vin} \rightarrow \text{Vout} \]

- Ideal digital
  \[ \frac{V_{dd}}{2}, V_{dd} \]

- Realistic
  \[ V_{in}, V_{out} \]

- Outside: slope = -1 points: change in Vin \rightarrow smaller change in Vout (wise suppression)

- Inside: \[ V_{in} \rightarrow \text{larger} \] ("amplify")

Stable 0 input: \[ 0V - V_{IL} \]

Stable 1 input: \[ V_{IH} - V_{dd} \]
All gates are cascaded

smallest normal input is \( V_{\text{OL}} \)
largest input is \( V_{\text{IH}} \)

One activity of Noise Margin

\[
N.M. \text{ Low} = V_{\text{IL}} - V_{\text{OL}}
\]
\[
N.M. \text{ HI} = V_{\text{OH}} - V_{\text{IH}}
\]

Space between normal input voltage and slope = -1 point

Summary:
- Keep a 0 a 0, and a 1 a 1
- Want to tolerate as much noise as possible
- Total noise \( \leq \) N.M. for proper operation
  \( = \) supply noise + crosstalk + ...

1) Process variation: transistor, wires
2) Voltage excursion: \( V_{\text{dd}} \)
3) Temp.
4) Noise

A) Generated external to chip
   - Power supply
   - Cosmic radiation

B) Generated internal to chip
   i) Inductive coupling

   \[ \begin{align*}
   &\text{Inductive coupling} \\
   &\text{Diagram of inductive coupling}
   \end{align*} \]

   ii) Capacitive coupling

   \[ \begin{align*}
   &\text{Capacitive coupling} \\
   &\text{Diagram of capacitive coupling}
   \end{align*} \]

   iii) Power and Gnd noise
      a) cycle-by-cycle

      \[ \begin{align*}
      &\text{Diagram of power and Gnd noise} \\
      &\text{Diagram of cycle-by-cycle noise}
      \end{align*} \]
b) longer period noise

Regeneration

A) Regenerative

B) Non-regenerative
To be regenerative, VTC has transient region with $|\text{gain}| > 1$

bordered by 2 zones with $|\text{gain}| < 1$

For all cases, $V_{in} = V_{out}$ @ $V_{in} = V_M$

\text{Fomout: # of gates connected to a gate's output}

Higher F.O. $\rightarrow$ a) driving gate gets slower

b) more "work" done

\text{Fomin: # of inputs to a gate. High Fomin: - more complex}

- more noise margin problems

+ more work done per gate
F04 - Format of 4

- a delay

- technology
- circuit size
  - inv
  - gates
  - functional units (+, -, x)
  - processor

Performance

\[ t_p = \text{average} = \frac{tpHL + tPLH}{2} \]

Rise & Fall times

Most commonly

10% < 90% of Vdd
Delay measurements
- depends on input rise/fall times
- depends on output loading
- Ring oscillator
  ![Ring Oscillator Diagram]
  Ex: F₀ = 1
  - odd # of invs
  - easier to measure freq than 20ps!
    light travels 6mm in 20ps!
  - other gates Ex:

Model inverter as:

![Inverter Diagram]
Vin → 0 → output via
Vdd-Vin → Load