Two ways to reduce probability:
1) small Rnwell & $R_{psub}$
2) reduce Vdd
   - reduce performance of circuit

1) nwell
   - surround all PMOS
   - typ. connected to Vdd
2) nwc - nwell contact

3) pwell
   - surround all NMOS
   - typ. connected to Gnd
4) pwc - pwell contact
Our magic file:

"=" see now well; see no well
"+" see no labels
"\" see "call"

Transfer Characteristics - Inverter

Ideal digital inverter
- \( \infty \) gain
- switching threshold \( \frac{V_{DD}}{2} \)

VTC - Voltage Transfer Characteristics

\[ \frac{V_{DD}}{2} \]
"Outside" slope = -1 \ points: change in \( V_{in} \) \( \rightarrow \) smaller change in \( V_{out} \) (noise suppressed)

"inside" \( \rightarrow \) larger \( \rightarrow \) larger \( \rightarrow \) noise amplified

Stable 0 Input: \( V_{0L} \leftrightarrow V_{IL} \)
Stable 1 Input: \( V_{1H} \leftrightarrow V_{OH} \)

One definition of noise margin:

\[
N.M._L = V_{IL} - V_{OL}
\]

\[
N.M._H = V_{OH} - V_{1H}
\]

Room between the normal input voltage and the slope = -1 point

- Want to tolerate as much noise as possible
- Keep a 0 a 0, keep a 1 a 1
- Total noise \( \leq N.M. \) for proper operation

\( \approx \) supply noise + cross talk + interference + ...
1) Process variation
   - Fast/slow transistors
2) Voltage variation (Vdd)
3) Temp variation
4) Noise
   a) Generated external to chip
      - Vdd
      - Cosmic radiation
   b) Generated internal to chip
      - Inductive coupling
      - Capacitive coupling
      - Power/grid noise
   - Cycle-by-cycle noise
- longer period noise

<table>
<thead>
<tr>
<th>CPU0</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>3</td>
</tr>
</tbody>
</table>

\[ \text{Vin} \rightarrow \text{Vout} \]

Regenerative VTO

\[ \text{Vin} \rightarrow \text{Vout} \]

Non-regenerative

\[ \text{Regenerative} \]

\[ \text{Non-regenerative} \]
**Fanout:** # of load gates connected to a gate's output

![Fanout diagram]

Higher fanout $\Rightarrow$ Slower gate delay
Move "work" done

**Famin:** # of inputs to a gate

![Famin diagram]

Higher fanin $\Rightarrow$ more complex gate
$\Rightarrow$ slower
$\Rightarrow$ more "work" done
$\Rightarrow$ generally more noise immunity, problems
For inverter

- Scales across:
  - PVT
  - fab. technologies
  - circuits: inv

Functional units \( (+, -, \times, \div) \)

Processors