In magic,

\[ \text{padm} 12 \text{c} \]
\[ \text{padm} 12 \text{c} \]
\[ \text{ndm} 12 \text{c} \]
\[ \text{pm} 12 \text{c} \]
\[ \text{m} 123 \text{c} \]
\[ \text{m} 234 \text{c} \]
\[ \text{m} 345 \text{c} \]
\[ \text{m} 456 \text{c} \]

4) Reduce Area

a) share, overlap (Ex: Vdd, Gnd)
Ex. 2 inverters

b) Abutment

Avoid bases of wires that turn corners, if possible

i) 

ii)
* (ii) 

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"pitch matching"

d) Consider shape of the overall structure

(i) 

(ii) 

*
For an arbitrary block, a square block will give the shortest total wire length.

e) Transistor folding (for large transistors)

+ large source cap

- large drain cap.

- may not fit SM cell

+ more source cap

+ less drain cap.
(6) Reducing max delay

\[ t_p = K \cdot R_{\text{mos}} \cdot C_{\text{load}} \]

- reduce \( R_{\text{mos}} \)
  - In layout, wider transistors
  - but this increases \( C_{\text{load}} \) for its driving gate
  - diminishing returns

- reduce \( C_{\text{load}} \)
  - shorter wires (lower \( L \))
  - reduce MOS width
  - smaller area
  - use higher-level metals if possible

(11) Reduce energy/operation

\[ P = C_L \cdot V^2 \cdot f \]
\[ E = C_L \cdot V^2 \]

* reduce \( C_L \)
  - \( Vdd \) and freq are generally set by other requirements
Latchup occurs when unintended parasitic bipolar transistors enter a state that shorts Vdd to Gnd.

Result:
- Positive feedback between NPN and PNP
- Locks up until power is turned off
- Device could overheat and melt
Avoid by:
- Small \( R_{\text{pwell}} + R_{\text{psub}} \)

\[ \rightarrow \text{keep well/sub contacts close to circuits} \]

\[ \rightarrow \text{116 rule:} \]

one nwell/psub contact every 3 "squares" of nwell or pwell