For an arbitrary block, a square will give the smallest total wire length and smallest area probably.

e) Transistor folding (for wide devices)

- May not fit into a short std. cell

- 1 schematic transistor
- 2 layout transistors

+ Source capacitance is larger (good)
+ Drain capacitance is reduced (good)
(10) Reduce max. delay

\[ t_p = K \cdot R_{\text{mos}} \cdot C_{\text{load}} \]

a) Reduce \( R_{\text{mos}} \)

- In layout, wider transistors
- but this makes \( C_L \) for driving gate larger
  
- helpful for under-driven nets
- in diminishing returns

b) Reduce \( C_{\text{load}} \)

shorter wire \( \rightarrow \) smaller area \( \rightarrow \) lower \( C_L \)

\[ \rightarrow \text{reduce } R_{\text{mos}} \text{ widths} \rightarrow \text{smaller area} \ldots \]

- use higher-level metals

(11) Reduce power

\[ P = C_L \cdot V_{dd}^2 \cdot \text{freq} \]

- \( V_{dd} \) is fixed, \( \text{freq} \) is fixed
  
- \( C_{\text{load}} \) - reduce it
- other techniques exist
Nwells, Pwells,

- nwell - surround all Nmos
  - generally connect to Vdd
  - nwc - "nwell contact"

  ![nwell_diagram]

- pwell - surround all NMOS
  - generally connect to Gnd
  - ignored for an nwell process

- pwc - pwell contact

  ![pwell_diagram]
Our `.mag/crc` file:

```
"=" see no nwell; see no pwell
"+" see no labels
"\"" see [all]
```

**Latchup**

Occur when unintended bipolar transistors enter a state
shorts `Vdd` and `Gnd`

![Diagram of latchup](image)

**Results:**
- Positive feedback between NPN and PNP
- Locks up until:
  - Power off
  - Overheats + melts
Avoid Latching:
- small $R_{psub}$ + $R_{nwell}$

* Small distance from MOS to $n_{wnc}$ $p_{wnc}$
- might reduce $V_{DD}$
  - will reduce speed

116 Rule: one $n_{wnc}/p_{wnc}$ every 3 "squares"
Ch. 5 - Inverter Characteristics

Vin → 0 → Vout

Vout is a function of Vin

- All inverters
  - Ideal digital inverter
    - 0 to gain
    - Switching threshold of Vdd/2
  - Realistic CMOS VTC

VTC curve
- Voltage transfer char.