In magic, all features are rectangles in a 2 x grid.
Contact and vias have very specific allowable sizes.

Cut see

Squares border size separation

Squares 09 18 36

**Layout Guidelines**

1. Vdd Orientation of Vdd + Gnd
   - Gnd

2. Stacking transistors

Better to share diffusions
+ smaller area
+ much smaller capacitance on node C
3) Orientation of transistors

* "vertically"
  + short poly

* "horizontally"
  + easy to make
  width transistors

4) Routing of Vdd/And

- in metal

* poly probably never

llb - unnecessary diffusion only for short distances

* - metal 1

  + very convenient for
  Vdd/And

* - metal 2

  + convenient for
  signals in/out
  of cell
- Use wider wires than min for Vdd / Gnd (> 6 x width)
- Use larger contacts than minimum

5. Rows of diffusion in a cell

* * Two

* * Row

- often has empty space

+ easier for complex cells

- hard to use with standard-height cells
6. Cell placement

- Place cells in alternating rows.

7. Metal routing discipline

Key Point: Every wire blocks perpendicular wires from using that layer.

a) Guideline: Try to use only m1 and m2 in small cells.

b) Guideline: Use only one direction for each layer.
c) Guideline: Alternate directions for each layer
   Ex: horizontal: (m1), m3, m5
       vertical: (m2), m4, m6

   Exception: ok to route ml and m2 any direction inside a cell to keep area small

   [Diagram of circuit layout]

   d) Guideline: Use lower metal for shorter wires
       "higher" "longer"
       (distance between vias)
(3) Stacked vias: to reduce area

Before CML, not possible to stack vias

Now with CML, we can stack vias

ml  m2  m3

ml  ml  m3