5) Rows of diffusion in a cell

a) Two

b) Four

- often have empty space
- better for complex cells
- hard to mix up 2-high cells

Generally avoid
6. Cell Placement

\[ \text{Vdd} \quad \text{Gnd} \]

\[ \text{Vdd} \quad \text{Gnd} \quad \text{Vdd} \quad \text{Gnd} \]

\[ \text{pwll/ndll} \quad \text{march/ldiff} \]

\[ \downarrow \]

\[ \text{pwll/ndll} \quad \text{row stripped} \]

7. Metal routing discipline

\[ \text{m1} \quad \text{m2} \quad \text{m3} \quad \text{m4} \quad \text{m5 or above} \]

Key point: Every wire blocks perpendicular wires from using that layer

a) Guideline: Try to use only m1 + m2 in small cells
b) **Guideline**: Use only one direction for each layer

Ex: (bad)

```
\[ m^4 \]
```

```
\[ \begin{array}{c}
    m^3 \\
    m^3
\end{array} \]
```

```
\[ \begin{array}{c}
    m^2 \\
    m^1
\end{array} \]
```

```
\[ \begin{array}{c}
    m^1 \\
    m^1
\end{array} \]
```

```
\[ \begin{array}{c}
    \text{Vdd} \\
    \text{Gnd}
\end{array} \]
```

c) **Guideline**: Use alternate directions for each layer

Ex. (horiz) (m1), m3, m5

(vert.) (m2), m4, m6

**Exception**: ok to route m1 + m2 any direction inside a cell

d) **Guideline**: Use lower metals for shorter wires, and higher metals for longer wires

* shorter and longer distance between vias

```
\[ \text{"short" wire} \]
```
Stack vias: to reduce area

Non-stackable vias: m1 - m3

Now, down to m0P, they can be stacked

Most advanced processes can stack arbitrarily high.

Magic:
- pm12c
- ncm12c
- pm12c
- m123c
- m234c
- m345c
- m456c

p diff, m1, m2
n diff, m1, m2
poly, m1, m2
m1, m2, m3

Remember that m2 is blocked.
(3) Reduce Area

a) Share, Overlay
   Ex. VDD, Gnd

   \[ \text{Ex. 2 invs} \]

   \[ \text{Gnd} \]

b) About

   \[ \text{Cont} \]

   \[ \text{Cin} \]
c) Avoid wires that turn corners, if possible

(i)  

(ii)  

* iii)  

* * iv)  

"pitch matching"
a) Consider shape of overall structure

Ex: 32-bit adder

i) worse

ii) better