Multi-Project Wafer (MPW) organizations

1) MOSIS
2) CMF - France
3) MUSE

Design Rules

Design File
- GDS II - binary - universally used
- CIF - text readable

Units
1) Absolute: μm, nm
2) Scalable: in magic, \( \frac{1}{2} \) min. feature size

\[ T_{500} = 0.19 \text{ nm} \quad \Rightarrow \quad \chi = 0.09 \text{ nm} = 90 \text{ nm} \]
We rules: Mosis "Smos DEEP"

1) min width of an object
2) min separation between 2 objects of same material
3) " " " " " different materials only

Manhattan - vertical + horizontal

- Dimensionless layout sketch
- Only topology is important
- Use magic colors
- Label nodes
- Draw contacts with "X"
II Layout Guidelines

1. Vdd / Gnd in schematics & layout

2. Stacking Transistors

   Better: "Share diffusion
   + smaller
   + lower cap - on "x"

3. Orientation of transistors

   - Tougher to stack
   + Easy to make wide transistors
Routing of VDD/ENA

- Always metal (diffusion only for short distances)

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  1) Metal 1
  - Most convenient for VDD/ENA
  - Common

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  2) Metal 2
  - Easy m1 connections outside cell

- Use wires wider than minimum (~6\(\lambda\))
- Try to use large (many) contacts