Photo masks

- Magic allows designers to work with logical layers
- Chip fab requires more details

Costs:
- 28nm $2M for mask set
- 14/16 nm $4M
- 7nm $8-10M

- Finer feature sizes
- Multiple pattern lithography (per layer)
Design Rules

Two main interfaces between chip designer + CMOS fab. engineer

1) Design Rules
2) Chip design file
   a) GDS II - binary format, universally used today
   b) CIF - text

"tape out" - design sent to fab

Units of design rules
1) absolute dimensions (\text{nm})
2) scalable design rules (\text{\(\lambda\)}) - magic

Common rules
1) min width of an object
2) min separation between 2 objects of same material
3) "" "" "" - different ""
\[ \lambda = \frac{1}{2} \text{ min. feature size} \]

\[ 0.18 \mu m \text{ CMOS } \Rightarrow \lambda = 0.09 \mu m \]

"SCMOS-DEEP" written by MOSIS

"Manhattan" layout

**Stick Diagrams**
- Dimensions
- Topology is important
- Two uses:
  - Useful intermediate step

[Diagram of stick diagram, schematic, layout]

- Automatic compaction tool
  - Not widely used
- Use colored pencils