Today

• Administrative items
  – Syllabus and course overview
  – Course objective and strategies

• My background

• Chapter 1

• Read Chapter 1


• Homework 1 posted on web page; due next Thursday
Teaching Assistants

• Ziyuan Dong

• Luis El Srouji

• Contact information is on the course web page
Course Workload

• 4 unit course
• Upper division
• This course requires significant effort and time
  – Circuits
  – Layout
  – Tools
    • Magic
    • Irsim
    • (Design Compiler, Innovus)
  – Major design project
Lectures and Labs

- Lectures
  - By zoom, links are on canvas
  - All lectures and exams

- Labs
  - In person
  - Wear masks at all times
    - cover your nose and mouth
    - the university takes this very seriously
  - Follow all instructions from your TA
    - https://campusready.ucdavis.edu/instructors

Student Responsibilities

Students are expected to:

- Monitor your symptoms and stay home if you are feeling sick. Take the Daily Symptom Survey to access campus facilities.

- Be fully vaccinated before the start of classes or hold an approved exception for religious or medical reasons. Additional time is granted to students who will have had no access to a vaccine before arriving on campus.

- Wear face coverings indoors and in mass transit. Unvaccinated students must also wear face coverings outdoors in crowded places.

- Test regularly as directed by campus guidelines. Testing is available at the ARC Testing Kiosk in Davis and at the Administrative Services Building in Sacramento. Students will face disciplinary action if they are out-of-date with testing requirements.

- Eat only in designated areas and never in classrooms. Students may remove their masks very briefly to drink while in class.
Lectures

• Ask questions at any time
  – Please raise your hand
  – Ask a question at any pause (zoom)

• Be respectful of others
  – Hold conversations outside of class
  – Silence phones
  – Sit in the back if you come in late or need to leave early
Course Communication

• In class during lecture
• Canvas announcements ➔ Email
  – Time-critical announcements only
• Web page
  – Primary source of course information
• Office hours
  – Posted on the course web page
  – Let me know by the second lecture if you have a conflict
• Please see me (or TA) in person or by zoom with questions rather than email
My Teaching Philosophy

• Primary goal (mine and yours): 
  *Learn VLSI design well*

• Achieve this through:
  – Reading textbook
  – Lectures
  – Solving problems on paper
  – Solving problems in lab
  – Discussions with other students, TA, myself
    • Come to office hours
Grading Philosophy

- Grading serves two main purposes:
  1. Motivate you to do the work required to learn
  2. Give others an indication of how well you know the material
    - Requires honest work and fair grading
Letter Grade Assignments

- I assign a letter grade only for the final course grade
- You can see score statistics for each graded item on Canvas
- I look at the final exams and course record of the class and assign two key dividing points: the A/A+ and D+/C- boundaries, and assign course grades from there using equally-sized intervals
  - No required numbers of any particular letter grades
  - Absolute scores are not important; the boundaries shift according to the difficulty of the exams in any quarter
  - In fact, easy exams cause large grade drops for small errors
  - Ignore any letter grades you might see on canvas
Working With Others

- **Collaboration**
  - Asking questions and explaining principles produces better work and dramatically increases learning
  - Working with others
    - Do homework and prelabs with classmates nearby
    - Ask each other questions, help each other—regarding *principles*, and *general approaches* to solving only
    - See *Course Collaboration Policy* on web page

- **Final Project: done individually**
  - Groups of 2

- **Dishonesty**
  - Copying produces similar work, stunts learning, is not fair to honest students, and is not allowed in this course
    - Students engaged in dishonest work will be referred to Student Judicial Affairs
    - I will try to keep in-class exams honest
    - Steps will be taken to keep out of class work honest
Penalties for Violating the *Policy on Student Conduct and Discipline*

- **Penalties**
  - Minimum penalty: meetings with SJA officer, zero grade on work, record with SJA
  - Permanent F grade on your transcript, no credit for the class
  - One to three quarter suspension from the university
  - Permanent dismissal from all ten campuses of the University of California. Permanent notation on your transcript.
Penalties for Violating the Policy on Student Conduct and Discipline

• Several perspectives
  – Personal obvious reasons
  – ECE and UCD (especially for those inclined to share work with someone doing poorly in class)
    Cheating harms our major and university’s reputation among employers who interview our graduates.

• In summary: The purpose of the penalties and this discussion is so that no one will get the penalty!!!
  Don’t do anything that violates the Policy on Student Conduct!
Penalties for Violating the *Policy on Student Conduct and Discipline*

• Typical scenario:
  – Someone shares code/design with another
  – They get caught
  – The “Copier” feels terrible guilt for causing a friend to get a zero
  – The “Sharer” deeply regrets sharing resulting in a zero when he/she should have had a full score
Exam and Quiz Regrades

• Some number of exams and quizzes will be scanned before being returned

• Key take-away messages:
  — Do not change anything on your work if you request a regrade
  — Students have in the past and got in big BIG trouble!!!
Cheating Websites
chegg, coursehero, etc.

• The university has recently taken a very strong stand against paying for work (2-quarter suspension for first offense in the last case)

• Key take-away messages:
  – Do not post assignments
  – Of course do not use any unpermitted outside material in work you submit
  – Of course do not post solutions
  – Two students did last year and got caught!!!
Submitting Work

• Unless announced otherwise, materials due must be submitted through canvas as instructed
• Only pdf format
  – It greatly simplifies grading
• Homework drop box on the second floor of Kemper
Course Web Page

http://www.ece.ucdavis.edu/~bbaas/116/

• This link is posted on the canvas home page
Colored pencils

- Buy colored pencils or pens whose colors match magic layout tool layer colors
  - green
  - brown (orange next closest?)
  - red
  - blue
  - purple
- Used for “stick diagrams”
- Slightly transparent pencils or pens work best
Areas of Research

- Processor architectures
  - Programmable
  - Special-purpose
- DSP algorithms
- Circuits
- VLSI design
- Software tools and applications

\[ G_c(m,n) = \alpha(m) \sum_{i=0}^{N-1} \alpha(n) \sum_{k=0}^{N-1} g(i,k) \cos \left( \frac{\pi(2k+1)n}{2N} \right) \cos \left( \frac{\pi(2i+1)m}{2N} \right) \]
Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2015 by K. Rupp
New data added by B. Baas
Moore’s Law – The number of transistors on integrated circuit chips (1971-2018)

Moore’s law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are linked to Moore’s law.

GC2: 16 nm, 23.6 billion transistors

The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic. Licensed under CC-BY-SA by the author Max Roser.
Processors Over Time

- Number of processors on a single die vs. year
- Each processor capable of independent program execution
Future Applications

- Very limited power budgets
- Require significant digital signal processing
Some Points on Course Coverage

• Emphasis on low-level design (full custom layout, circuits). EEC 180 is higher-level

• Emphasis on VLSI-specific issues
  – Coverage of CMOS fabrication technology

• Focus on digital circuits rather than analog circuits
  – Due to tremendous simplifications in circuit design, layout extraction, and simulation

• Limited coverage of digital circuits such as what is covered in EEC 118
EEC 116 Outline

- Introduction
- Cost, yield
- CMOS fabrication
- CMOS VLSI layout
- Inverter characteristics
- MOS resistance, capacitance
- Sequential circuits
- Optimizing performance
- Complex combinational gates
- Logic circuit styles
- Wires
- Chip-level structures
- Chip-level issues
- Array memories
- Packaging
- Standard cell P&R overview
Chapter 1—Introduction

- History of computing
- What is inside a processor
- How they are designed
The First Computer

The Babbage Difference Engine (1832)

25,000 parts

cost: £17,470

Source: Digital Integrated Circuits, 2nd ©
ENIAC - The first electronic computer (1946)

Source: Digital Integrated Circuits, 2nd ©
What Is A Processor?

• Something that processes!

Example applications:
– Microwave oven controller
– CD or DVD player
– Hearing aid
– Personal computer
– Digital watch
– Cell phone
– Radar for an airplane
– Datacenter server processor
What Is Inside One?

- Three main components
  - Memory
What Is Inside One?

• Three main components
  – Memory
  – Datapath
What Is Inside One?

• Three main components
  – Memory
  – Datapath
  – Control
Memory

- Stores information
- Examples
  - Temporary chip memory
    - "256 MB RAM"
  - Permanent chip memory
    - "Flash non-volatile memory"
  - Hard disk
    - "80 GB disk"
Datapath

- Processes information
- Example tasks
  - Add
  - Multiply
  - Move
  - Compare
Control

• Runs the show

• Examples
  – Software
    • Word, Excel
    • Large database
  – Hardware (best for simpler, fixed, high-speed tasks)
    • MP3 player
    • Signal processing
Simple Blocks Working Together
Example #1

- Auto cruise control
  - Watch car’s speed \((input)\)
  - Compare with set speed \((datapath, compare)\)
  - If adjustment is needed, add or subtract \((datapath)\) from setting and send update to gas pedal \((output)\)
Simple Blocks Working Together
Example #2

- Google search
  - Type in search words (*input*)
  - Look through large database of web pages (*memory*) until matches are found (*datapath, compare*)
  - When list is found, send it to user (*output*)
Simple Blocks Working Together

• **Key point**
  – Simple operations alone can not do much, but billions of simple operations per second can do a lot!
How Large Are Transistors?

- If a human hair were this large...

- A transistor that was state of the art around the year 2002 (0.18 µm) would be this long

- Modern transistors are approximately 35× smaller...

Source: Richard Spencer
The First Transistor

- Fabricated at Bell Labs on December 16, 1947. The inventors William Shockley, John Bardeen, and Walter Brattain won the Nobel prize in physics in 1956 for the invention. It is one of the most important inventions in history.
The First Integrated Circuit

- This is the first IC made by Jack Kilby of Texas Instruments. It was built in 1958.

Source: Richard Spencer
An Early “Planar” IC

- This is an early planar IC from Fairchild.

Source: Richard Spencer
Intel 4004
The First Single-Chip Microprocessor

- released in 1971
- 2,250 transistors
- 10 µm minimum feature size
- 0.75 MHz max clock rate

[Digital Integrated Circuits, 2nd © ; wikipedia]
Intel Pentium 4 Microprocessor

- Introduced in 2000
  - 42 million transistors
  - 0.18 µm CMOS

Source: Intel
http://www.intel.com/museum/online/hist_micro/hof/
Nvidia
Kepler
GK110

- 7.1 Billion transistors
- 2880 CUDA datapaths

Source: xxxxxxx

EEC 116, B. Baas
Silicon

- Silicon is the second most common element in the Earth’s crust.
- Semiconductor-grade Si is 99.999999 % pure.
- Ingots like this one weigh several hundred pounds and cost $16,000
- The ingot will be sliced into very thin wafers.
A Silicon Wafer

- This 8-inch wafer contains about 200 Pentium II chips (1997).
- Each chip contains more than 20 million transistors.
- More than 1 billion microprocessors are made each year.

Source: Richard Spencer
A State-of-the-art Wafer

• 300 mm diameter wafer
Wires

- Four levels of wires shown here
- Designers specify each layer and connections between layers

Source: IBM
Chip Wires

• Modern chips have up to 13+ layers of wires

Source: IBM
Chip Wires
Memory Array

- Human hair on a 256 Kbit memory chip

Source: Helmut Föll
Memory Array

- Human hair on a 4 Mbit memory chip
- Note DRAM trench capacitors

Source: Helmut Föll
Memory Array

- Red blood cells on a 1 Mbit memory chip

Source: Helmut Föll