Today

• Administrative items
  – Syllabus and course overview
  – Course objective and strategies

• My background

• Chapter 1

• Read Chapter 1


• Homework 1 posted on web page; due next Thursday
Teaching Assistants

- Ziyuan Dong
- Zhangfan Zhao
- Contact information is on the course web page
Course Workload

• 4 unit course
• Upper division
• This course requires significant effort and time
  – Circuits
  – Layout
  – Tools
    • Magic
    • Irsim
    • (Design Compiler, Innovus)
  – Major design project
Course Communication

• Email list
  – Urgent announcements

• Web page
  – Primary source of course information

• Office hours
  – Tue 4:30 after lecture
  – Th 4:30 after lecture
  – Tentatively: Mon 2-3pm

• Please see me (or TA) in person with questions rather than email
Lectures

• Ask questions at any time
  – Please raise your hand or in zoom speak out

• Be respectful of others
  – Hold conversations outside of class
  – Silence phones
  – Sit in the back if you come in late or need to leave early
My Teaching Philosophy

• Primary goal (mine and yours):
  
  *Learn VLSI design well*

• Achieve this through:
  – Reading textbook
  – Lectures
  – Solving problems on paper
  – Solving problems in lab
  – Discussions with other students, TA, myself
    • Come to office hours
My Grading Philosophy

• Grading serves two main purposes:
  – 1. Motivate you to do the work required to learn
  – 2. Give others an indication of how well you know the material
    • Requires honest work and fair grading
Letter Grade Assignments

- I assign a letter grade only for the final course grade
- You can see score statistics for each graded item on Canvas
- I look at the final exams and course record of the class and assign two key dividing points: the A/A+ and D+/C- boundaries, and assign course grades from there using equally-sized intervals
  - No required numbers of any particular letter grades
  - Absolute scores are not important; the boundaries shift according to the difficulty of the exams in any quarter
  - In fact, easy exams cause large grade drops for small errors
  - Ignore any letter grades you might see on canvas

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(not actual grade data)
Working With Others

• Collaboration
  – Asking questions and explaining principles produces better work and dramatically increases learning
  – Working with others
    • Do homework and prelabs with classmates nearby
    • Ask each other questions, help each other — regarding principles, and general approaches to solving only
    – See Course Collaboration Policy on web page

• Final Project: done individually
  – Groups of 2

• Dishonesty
  – Copying produces similar work, stunts learning, is not fair to honest students, and is not allowed in this course
    • Students engaged in dishonest work will be referred to Student Judicial Affairs
    • I will try to keep in-class exams honest
    • Steps will be taken to keep out of class work honest
Penalties for Violating the Policy on Student Conduct and Discipline

• Penalties
  – Minimum penalty: meetings with SJA officer, zero grade on work, record with SJA
  – Permanent F grade on your transcript, no credit for the class
  – One to three quarter suspension from the university
  – Permanent dismissal from all ten campuses of the University of California. Permanent notation on your transcript.
Penalties for Violating the *Policy on Student Conduct and Discipline*

• Several perspectives
  – Personal obvious reasons
  – ECE and UCD (especially for those inclined to share work with someone doing poorly in class)
    Cheating harms our major and university’s reputation among employers who interview our graduates.

• In summary: The purpose of the penalties and this discussion is so that no one will get the penalty!!! Don’t do anything that violates the Policy on Student Conduct!
Penalties for Violating the *Policy on Student Conduct and Discipline*

- Typical scenario:
  - Someone shares code/design with another
  - They get caught
  - The “Copier” feels terrible guilt for causing a friend to get a zero
  - The “Sharer” deeply regrets sharing resulting in a zero when he/she should have had a full score
Exam and Quiz Regrades

• Some number of exams and quizzes will be scanned before being returned

• Key take-away messages:
  – Do not change anything on your work if you request a regrade
  – One student did last year and got in big BIG trouble!!!
Cheating Websites
chegg, coursehero, etc.

• The university has recently taken a very strong stand against paying for work (2-quarter suspension for first offense last year)

• Key take-away messages:
  – Do not post assignments
  – Of course do not use any unpermitted outside material in work you submit
  – Of course do not post solutions
  – Two students did last year and got caught!!!
Submitting Work

• Unless announced otherwise, materials due on lecture days are due at the beginning of class
• Submit work through canvas as instructed
• Homework drop box on the second floor of Kemper
Course Web Page

http://www.ece.ucdavis.edu/~bbaas/116/
Colored pencils

- Buy colored pencils or pens whose colors match magic layout tool layer colors
  - green
  - brown (orange next closest?)
  - red
  - blue
  - purple
- Used for “stick diagrams”
- Slightly transparent pencils or pens work best
Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten

New plot and data collected for 2010-2015 by K. Rupp

New data added by B. Baas
Moore’s Law – The number of transistors on integrated circuit chips (1971-2018)

Moore’s law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are linked to Moore’s law.

The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.
Processors Over Time

- Number of processors on a single die vs. year
- Each processor capable of independent program execution
Processor Eras

- **Transistor Era:** the Intel 4004 was the first commercial single-chip microprocessor and it contained 2300 hand-drawn transistors.

- **Single/Multi-Processor Era:** focus on components of single processors and multi-processors, which generally scale well to only small numbers of processors.

- **1000-Processor Era:** focus on making systems scalable and working with processors as building blocks. The KiloCore design would contain approximately **140,000 independent MIMD processors** in 14 nm if its area were the same as the 12 nm 815 mm^2 Nvidia GV100.
- Processors drawn approximately to scale based on incomplete data
- Consider for each processor tile: maximum wire length $\propto$ capacitance $\propto$ energy
- Consider for each processor tile: circuit overhead per operation
Undergraduate Research

• Talk to me if you are interested!
• I will say that there is a very strong correlation with GPA and success in research
Future Applications

• Very limited power budgets
• Require significant digital signal processing
Some Points on Course Coverage

- Study of CMOS fabrication technology only
- Focus on digital circuits rather than analog circuits
  - Due to tremendous simplifications in circuit design, layout extraction, and simulation
- Emphasis on low-level design (full custom layout, circuits). EEC 180B is higher-level
- Emphasis on VLSI-specific issues
- Limited coverage of digital circuits such as what is covered in 118
EEC 116 Outline

- Introduction
- Cost, yield
- CMOS fabrication
- CMOS VLSI layout
- Inverter characteristics
- MOS resistance, capacitance
- Sequential circuits
- Optimizing performance
- Complex combinational gates

- Logic circuit styles
- Wires
- Chip-level structures
- Chip-level issues
- Array memories
- Packaging
- Standard cell P&R overview
Chapter 1—Introduction

• History of computing
• What is inside a processor
• How they are designed
The First Computer

The Babbage
Difference Engine
(1832)

25,000 parts
cost: £17,470

Source: Digital Integrated Circuits, 2nd ©
ENIAC - The first electronic computer (1946)
How Large Are Transistors?

- If a human hair were this large...

A transistor that was state of the art around the year 2002 would be this long...

Source: Richard Spencer
The First Transistor

- Fabricated at Bell Labs on December 16, 1947. The inventors won the Nobel prize in physics in 1956 for the invention.

Source: Richard Spencer
The First Integrated Circuit

- This is the first IC made by Jack Kilby of Texas Instruments. It was built in 1958.

Source: Richard Spencer
An Early “Planar” IC

• This is an early planar IC from Fairchild.

Source: Richard Spencer
Intel 4004 Micro-Processor

1971
1000 transistors
1 MHz operation

Source: Digital Integrated Circuits, 2nd ©
Intel Pentium 4 Microprocessor

- Introduced in 2000
  - 42 million transistors
  - 0.18 µm CMOS

Source: Intel
http://www.intel.com/museum/online/hist_micro/hof/
Nvidia Kepler GK110

- 7.1 Billion transistors
- 2880 CUDA datapaths

Source: xxxxxxx

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Silicon

- Silicon is the second most common element in the Earth’s crust.
- Semiconductor-grade Si is 99.999999 % pure.
- Ingots like this one weigh several hundred pounds and cost $16,000.
- The ingot will be sliced into very thin wafers.
A Silicon Wafer

• This 8-inch wafer contains about 200 Pentium II chips (1997).
• Each chip contains more than 20 million transistors.
• More than 1 billion microprocessors are made each year.

Source: Richard Spencer
A State-of-the-art Wafer

- 300 mm diameter wafer

Source: IBM
Wires

- Four levels of wires shown here
- Designers specify each layer and connections between layers

Source: IBM
Chip Wires

- Modern chips have up to 13+ layers of wires

Source: IBM
Chip Wires

Source: IBM
Memory Array

- Human hair on a 256 Kbit memory chip

Source: Helmut Föll
Memory Array

- Human hair on a 4 Mbit memory chip
- Note DRAM trench capacitors

Source: Helmut Föll
Memory Array

- Red blood cells on a 1 Mbit memory chip

Source: Helmut Föll
Transistor Layout

• Drawing a transistor is this easy!

PMOS transistor

NMOS transistor
AND Gate Layout

- Here is an AND gate (with an inverted output, which is called a NAND)
• Here is an OR gate (with an inverted output, which is called a NOR)
Here is a Full Adder

Source: Mike Lai
16-bit Adder Layout

- Here is a complete 16-bit adder (it adds two numbers where each input can range from \(-32,000\) to \(+32,000\))
- This adder contains 16 full adders (essentially) plus additional circuits for fast addition

Source: Mike Lai
16-bit Multiplier Layout

- Here is a complete 16-bit x 16-bit multiplier (each input can range from \(-32,000\) to \(+32,000\))

Source: Mike Lai