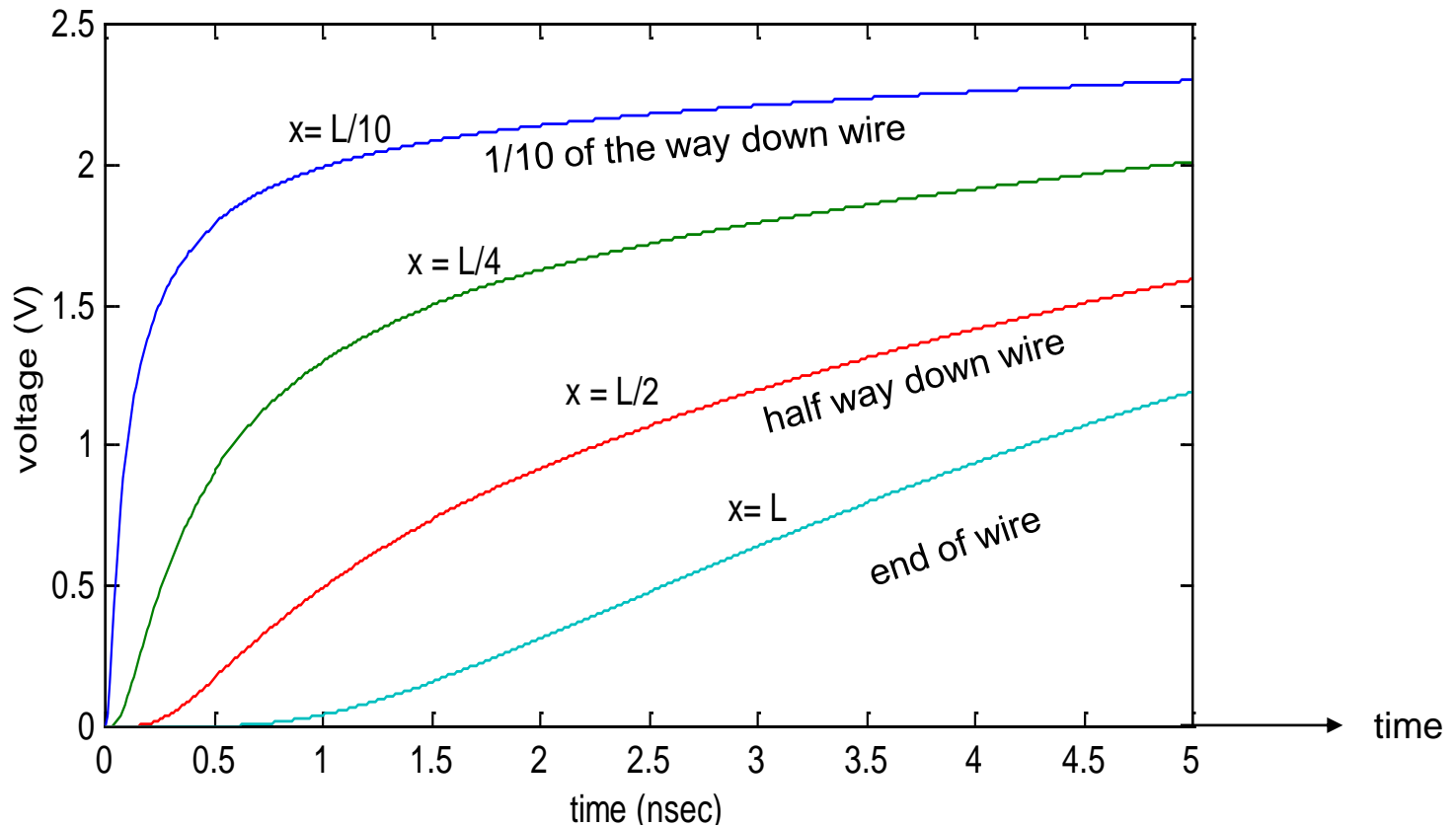


Comparison of 3 Interconnect Layers

Interconnect over Field	Capacitance Parallel Plate	Capacitance Fringe	Capacitance Parallel + Fringe	Capacitance Inter-Wire @ minimum space
poly – <i>field</i>	88 aF/ μm^2 = 22 aF/μm length with 0.25 μm wide wire	54 aF/ μm length for 1 side	130 aF/ μm length	40 aF/ μm length
Al M1 – <i>field</i>	30 aF/ μm^2 = 11 aF/μm length with 0.38 μm wide wire	40 aF/ μm length for 1 side	91 aF/ μm length	95 aF/ μm length
Al M5 – <i>field</i>	5.2 aF/ μm^2 = 2.6 aF/μm length with 0.50 μm wide wire	12 aF/ μm length for 1 side	27 aF/ μm length	115 aF/ μm length (2 \times thicker than M1)

- As expected, higher levels of interconnect have lower capacitance per area
- Inter-wire capacitance can be greatly reduced with increased spacing

Step-response of an RC Wire as a Function of Time and Space (Fig. 4-15, p. 157)



Ways to Reduce Wire Delays

- $t_p = k r c L^2$
Recall wire propagation delay is a function of its length squared
So efforts in making wires shorter has a large benefit when wire delays are significant
- 1) Make wire shorter – using good layout techniques
- 2) Possibly increase width of wire
 - Most useful with highly resistive interconnect like polysilicon
- 3) Increase intra-layer wire spacings
 - $C = \epsilon (A / t)$
- 4) Use a routing layer with lower resistance and lower capacitance such as a higher level of metal

Ways to Reduce Wire Delays

5) Pipeline circuit

- Signal would then arrive in a later cycle which would require architectural changes and may not be acceptable

6) Insert repeaters along length of wire

- Ex: wire of length L

Delay with a single wire of length L : $k r c L^2$

Delay if wire is divided into 3 segments by adding two inverters

$$= 3 \times (k r c (L/3)^2) + (2 \times \text{Delay}_{\text{inverter}})$$

$$= (k r c L^2) / 3 + (2 \times \text{Delay}_{\text{inverter}})$$

Design Rules of Thumb

- rc delays should be considered when

1) $t_{p\text{-wire}RC} \gg t_{p\text{-gate}}$ of the driving gate.

critical length of wire = L_{crit}

consider wire rc delay when $L_{crit} \gg \sqrt{t_{pgate}/0.38rc}$

2) the rise (fall) time at the line input is smaller than RC , the rise (fall) time of the line

$$t_{rise} \text{ or } t_{fall} < RC$$

Transmission Lines

- Transmission line modeling needed when
 - Time of flight across a wire comparable to the rise/fall times
 - Signal moves as a wave across the wire
 - Think of a wave moving across a swimming pool
 - It can bounce back—off a wall for example
- Lossless transmission line
 - signal velocity $v = 1 / \sqrt{lc}$; l =inductance per length, c =capacitance per length
 - $t_p = 1/v = \sqrt{lc}$
 - characteristic impedance of the wire
 - $Z_0 = \sqrt{l/c}$

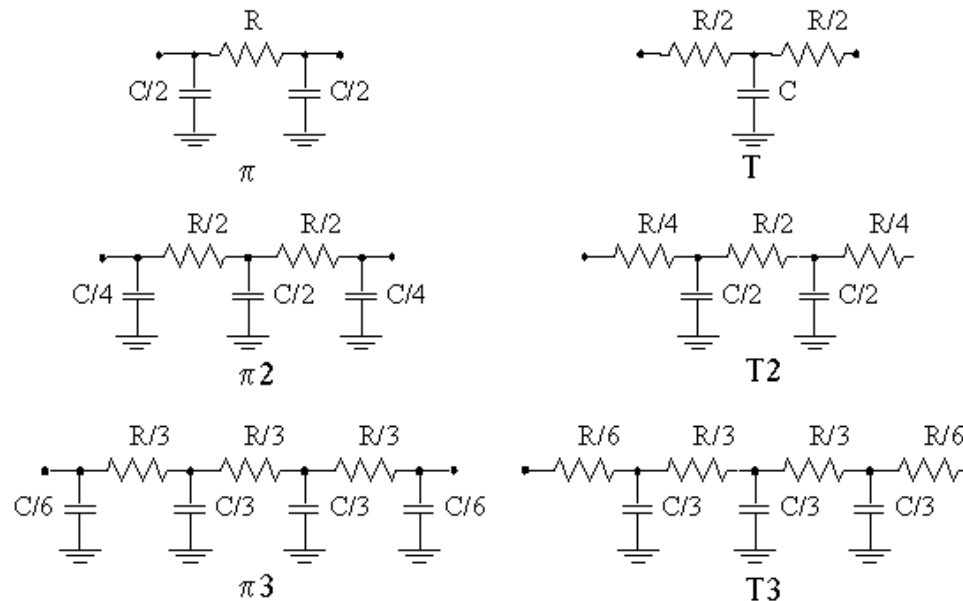
Transmission Lines

- Typical on-chip characteristic impedances 10 – 200 ohms
- Best performance (no reflections) requires the wire is terminated
 - termination impedance = characteristic impedance

RC-Models

Voltage Range	Lumped RC-network	Distributed RC-network
0→50% (t_p)	0.69 RC	0.38 RC
0→63% (τ)	RC	0.5 RC
10%→90% (t_r)	2.2 RC	0.9 RC

Step Response of Lumped and Distributed RC Networks:
Points of Interest.



Research In Wires: Graphene

Move Over Graphene: IBM Expects Copper Interconnects to Hold the CMOS Line ExtremeTech, November 16, 2017

“It’s been 20 years since IBM first introduced copper interconnects in CMOS processing, sparking a minor revolution in the process. Within a handful of years, both Intel and AMD had made the jump as well, paving the way for reduced interconnect power consumption and improved performance when compared with the older aluminum interconnect standard. Now, IBM believes there’s enough life left in copper — and enough problems with graphene — that copper-based interconnects will last until CMOS is itself replaced by something new.

“... IBM fellow Dan Edelstein...argues graphene is too difficult to manufacture, doesn’t flow uniformly, and doesn’t achieve the same consistent performance as modern copper interconnects. ... No one has yet found a cost-effective way of manufacturing graphite at scale or of manufacturing it to the tolerances required.

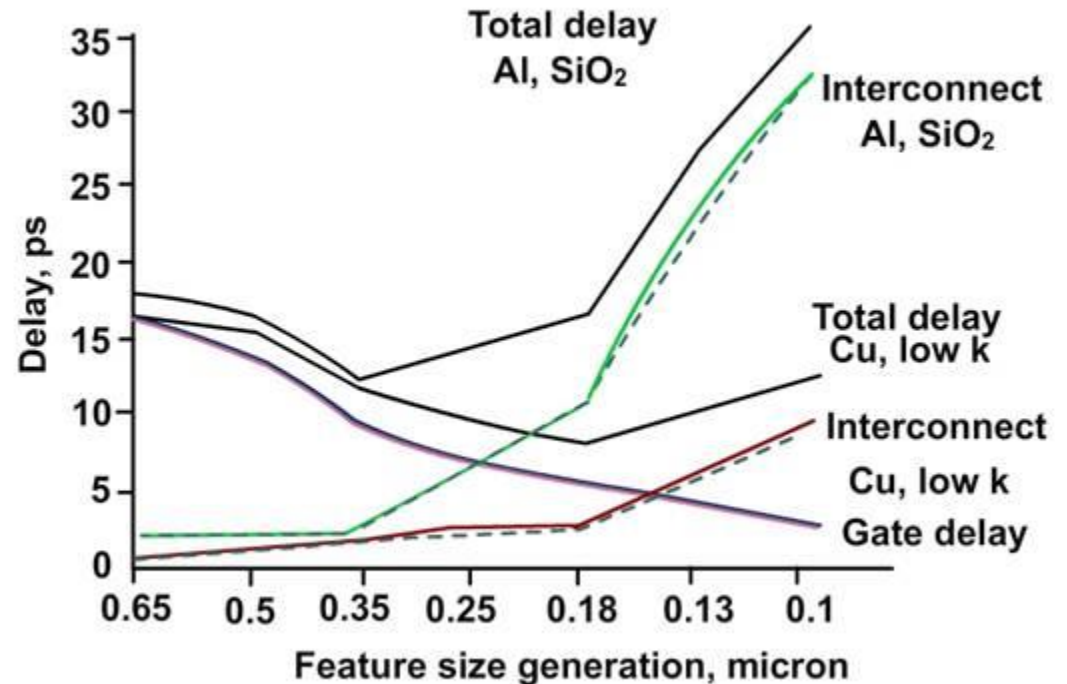
“Copper with a thin cap of cobalt is better than graphene at carrying current and even at the smallest sizes imaginable copper interconnects are still the best solution, perhaps with cobalt, nickel, ruthenium or another platinum-group noble metals brought in to underlay it,” Edelstein said.

Research In Wires: Graphene

Move Over Graphene: IBM Expects Copper Interconnects to Hold the CMOS Line ExtremeTech, November 16, 2017

“Copper offered significant benefits over aluminum, as shown in the image [right], but it also required a tantalum-nitride sheath to act as a diffusion barrier between copper ions and the silicon itself. IBM had to develop entirely new methods of connecting the various layers of the CPU; the techniques that had worked well for aluminum did not function for copper.

“At first our competitors said that it would only last one generation, but so far it has lasted 12,” Edelstein told EETimes.



Research In Wires: Graphene

Move Over Graphene: IBM Expects Copper Interconnects to Hold the CMOS Line ExtremeTech, November 16, 2017

“ ‘And we believe that for CMOS it will last forever, except perhaps on the bottom layer next to the advanced node silicon transistors which may require cobalt, nickel, ruthenium or another platinum-group noble metals.’

“As semiconductor nodes have become smaller, interconnect delay has risen and become an increasingly difficult problem to solve. It’s part of the reason why CPU clocks haven’t advanced much. We need a better interconnect solution, no question, but so far, we simply haven’t found one. The problems facing graphene are significantly more difficult than the issues that made copper integration difficult in the 1990s, and until we can actually produce the stuff in the commercial volumes required for mainstream manufacturing, it wouldn’t matter if it was the best interconnect material on Earth.”