PACKAGING

IC Packaging

- Purposes
  1) Electrical connections
     - Signals
     - Power and ground
  2) Aids heat dissipation
     - Increase effective surface area for increased convection
     - Heat conduction into PC board
  3) Physical protection for IC
     - e.g., against breakage
  4) Environmental protection
     - Hermetic (airtight) seal
     - e.g., against corrosion or moisture

Rent's Rule

- Empirical formula
- $P = K\, G^{\beta}$
- P = number of input/output connections (pins)
  K = average number of I/Os per "gate"
  G = number of "gates"
  β = empirically-found parameter that varies according to application; generally between 0.1 and 0.7

	β	K
Computer (chip)	0.63	1.4
Computer (board)	0.25	82
Static memory	0.12	6

Package Metrics

- Electrical
  - Low capacitance
  - Low inductance
  - Low resistance
- Mechanical
  - Reliable across temperature variations (thermal expansion matching)
- Thermal
  - Low thermal resistance to get the heat out
- Economical (cost)
  - Purchase of package
  - Assembly (chip and board assembly)
  - System (heat removal equipment included)

Package Materials

- Plastic
  - Low cost
  - Typically requires a custom-designed package
- Ceramic
  - Better heat transfer characteristics
  - Generally more reliable
  - More likely an off-the-shelf part can be used
    - Good for research and prototyping

Interconnection Levels

- Multiple levels of packaging
  - Ease of handling
  - Reuse of intermediate-sized modules (e.g., DRAM memory stick)
    - Use in multiple products
    - Upgradeable in field
    - Repairable in field

system

printed circuit board(PCB)

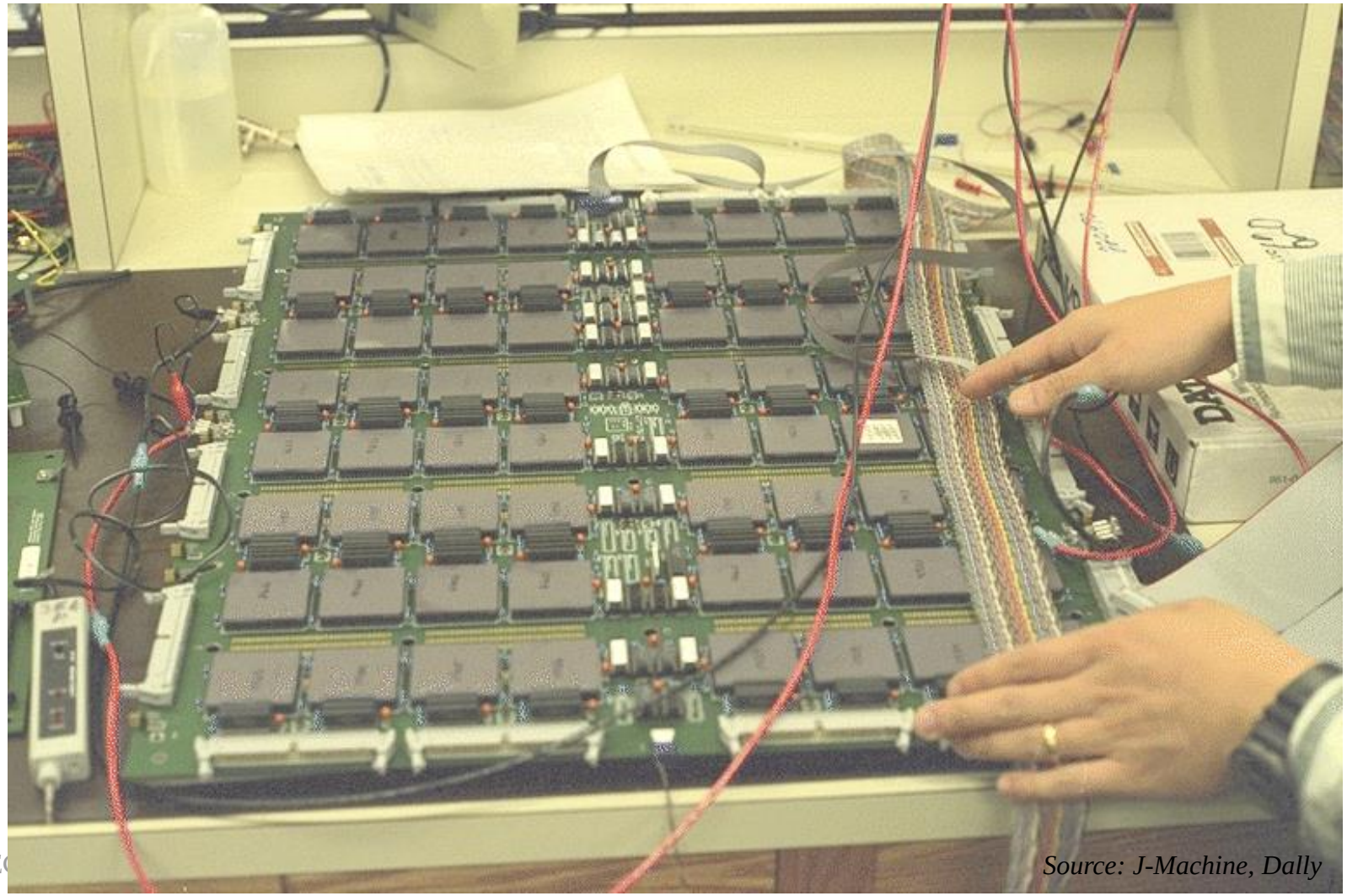
package

chip

Solder

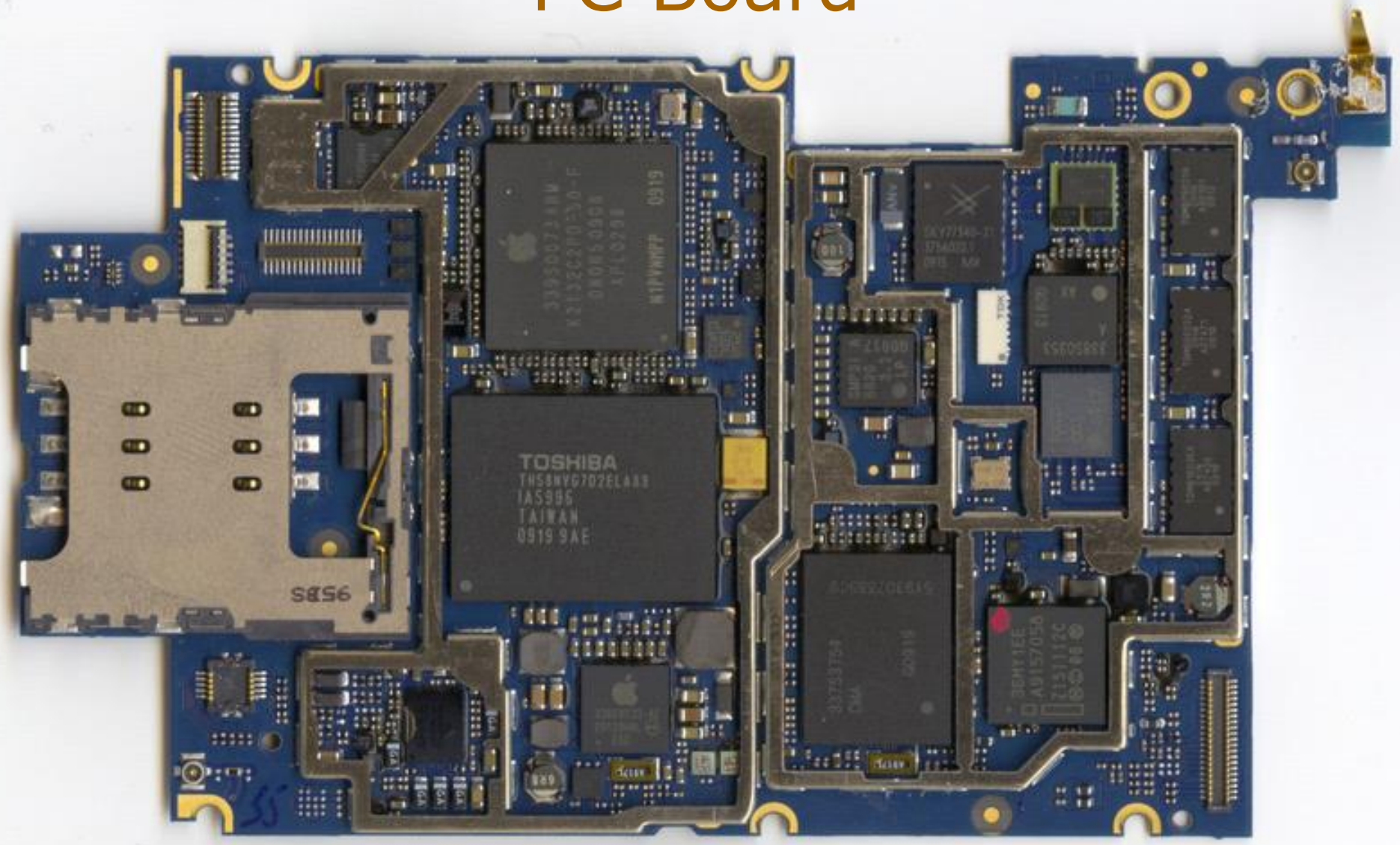
- Solder is the universal electrical "glue"
  - tin and lead alloy: 50/50%, 63/37% Sn/Pb eutectic mixture
  - low melting temperature: 183 °C or 361.4 °F for eutectic
  - good electrical conductivity
- Large efforts now under way to eliminate or reduce the use of lead
  - RoHS - Restriction of Hazardous Substances Directive
  - Many replacements available
    - Typical ones use Tin, Silver, Copper; maybe Bismuth, Indium, Zinc, Antimony

PC Board



Source: J-Machine, Dally

PC Board



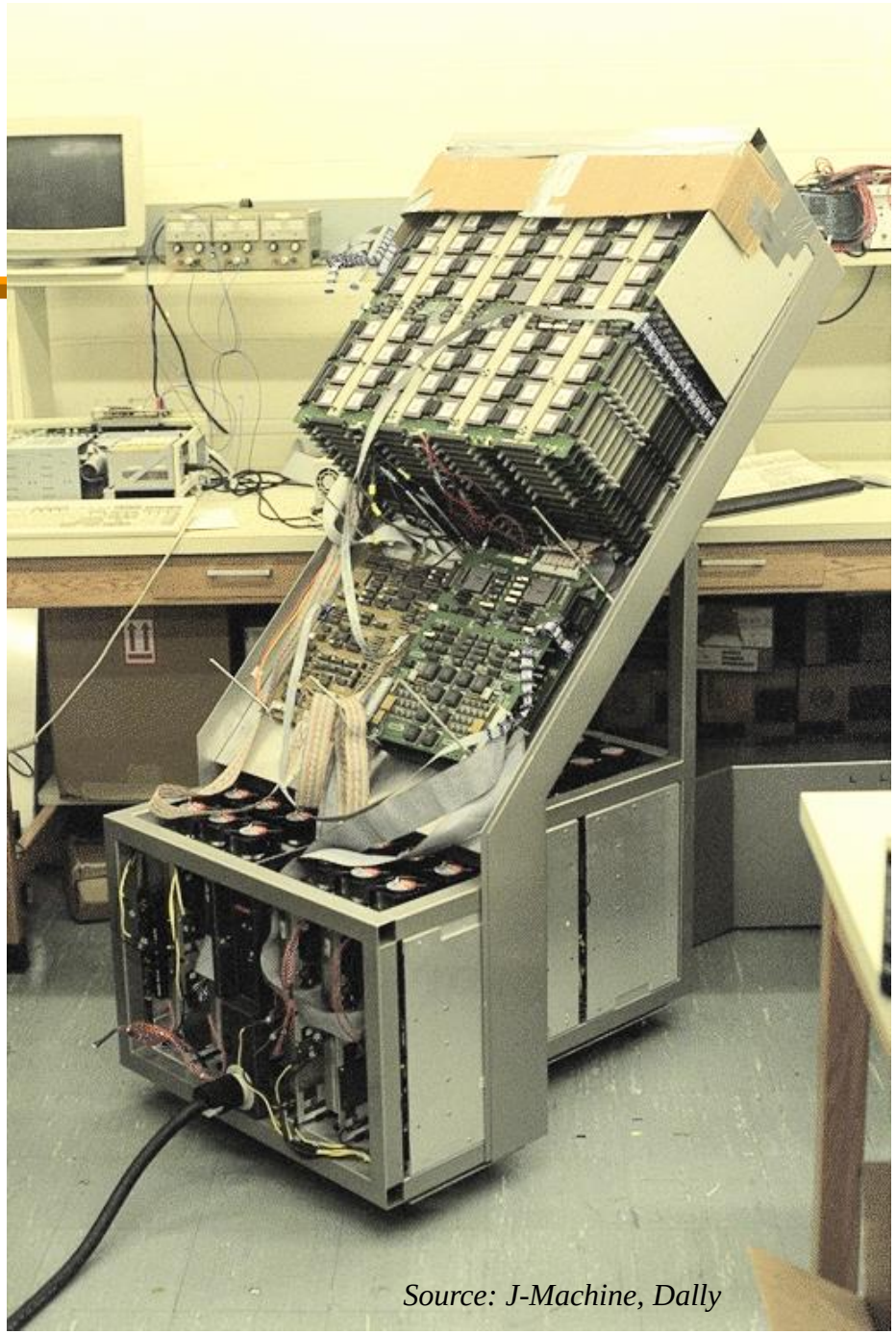
iPhone 3GS, AppleInsider, June 19, 2009

PC Board Stack With Host Computer

Source: J-Machine, Dally

System

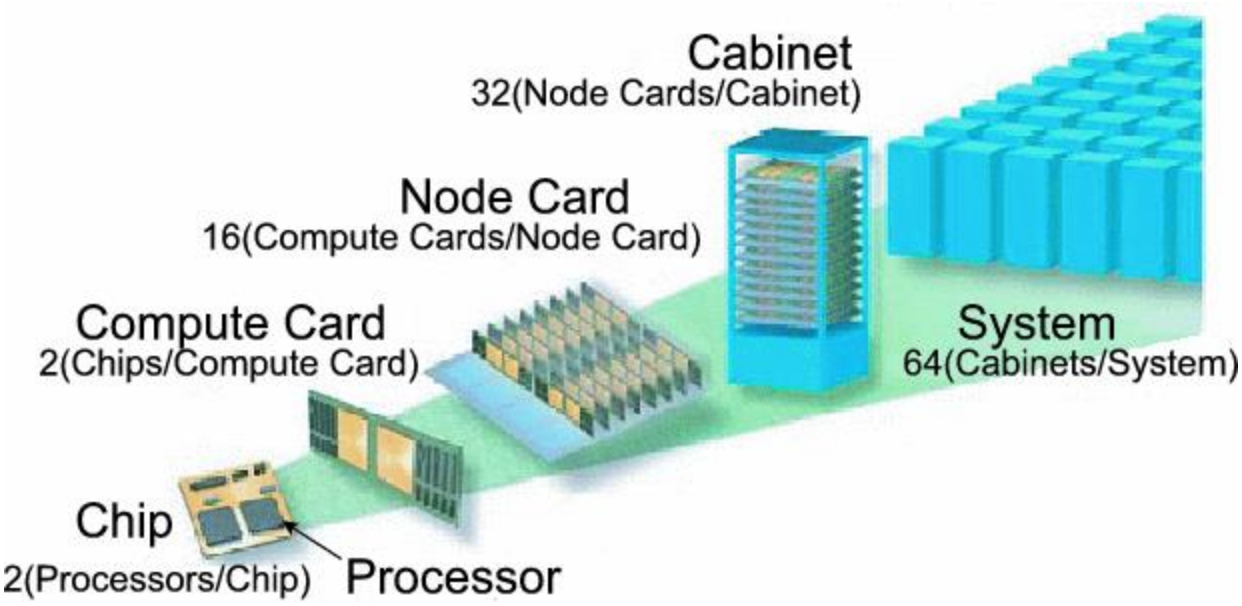
- J-Machine
- Built at MIT and Stanford in the early 1990's
- 1024 processors



Source: J-Machine, Dally

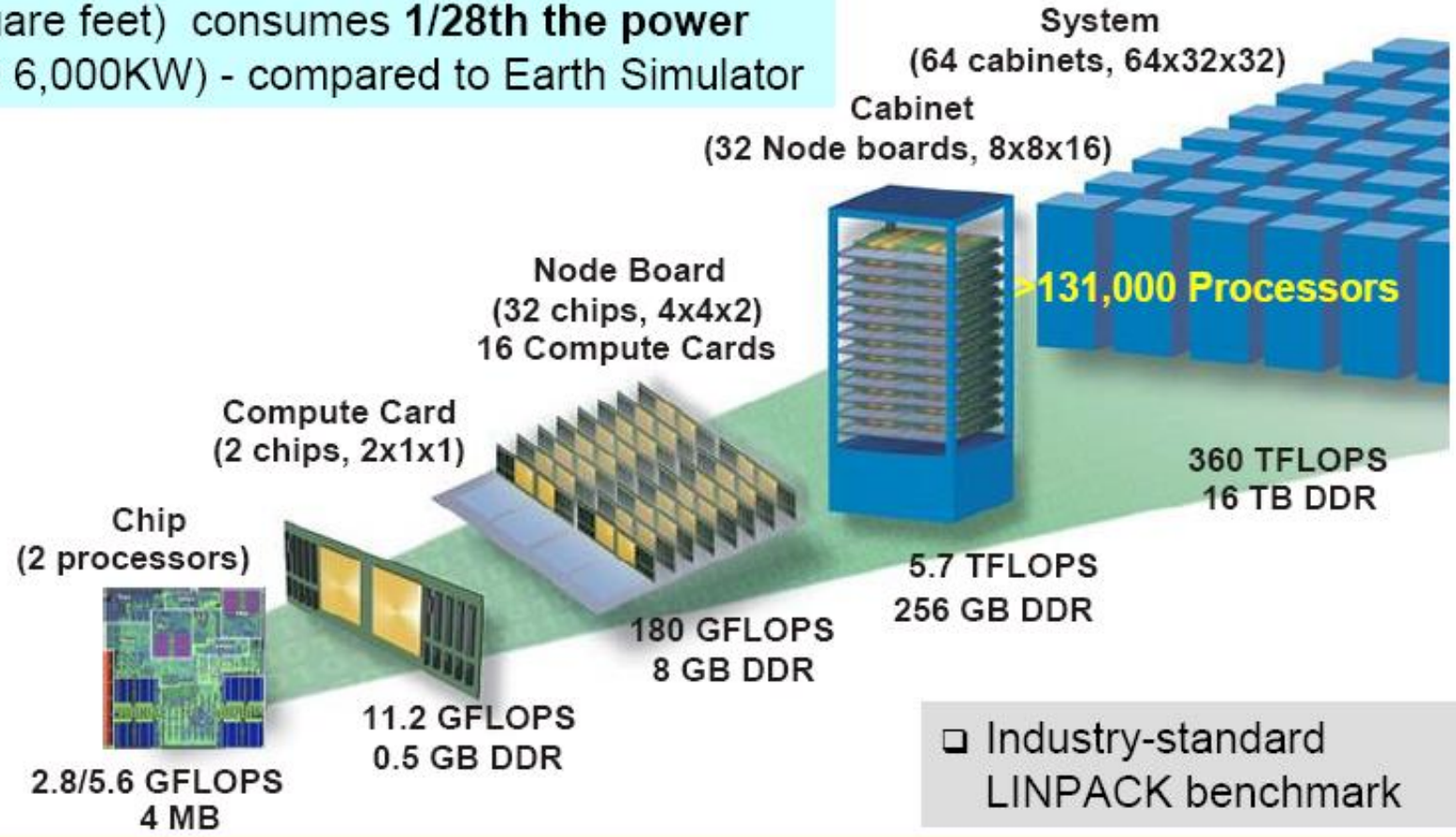
IBM Blue Gene/L

- A formerly-fastest supercomputer in the world is a 131,072-processor Blue Gene machine



IBM Blue Gene/L

- **BlueGene/L**: **1/100th the physical size** (320 vs 32,500 square feet) consumes **1/28th the power** (216KW vs 6,000KW) - compared to Earth Simulator



- Industry-standard LINPACK benchmark

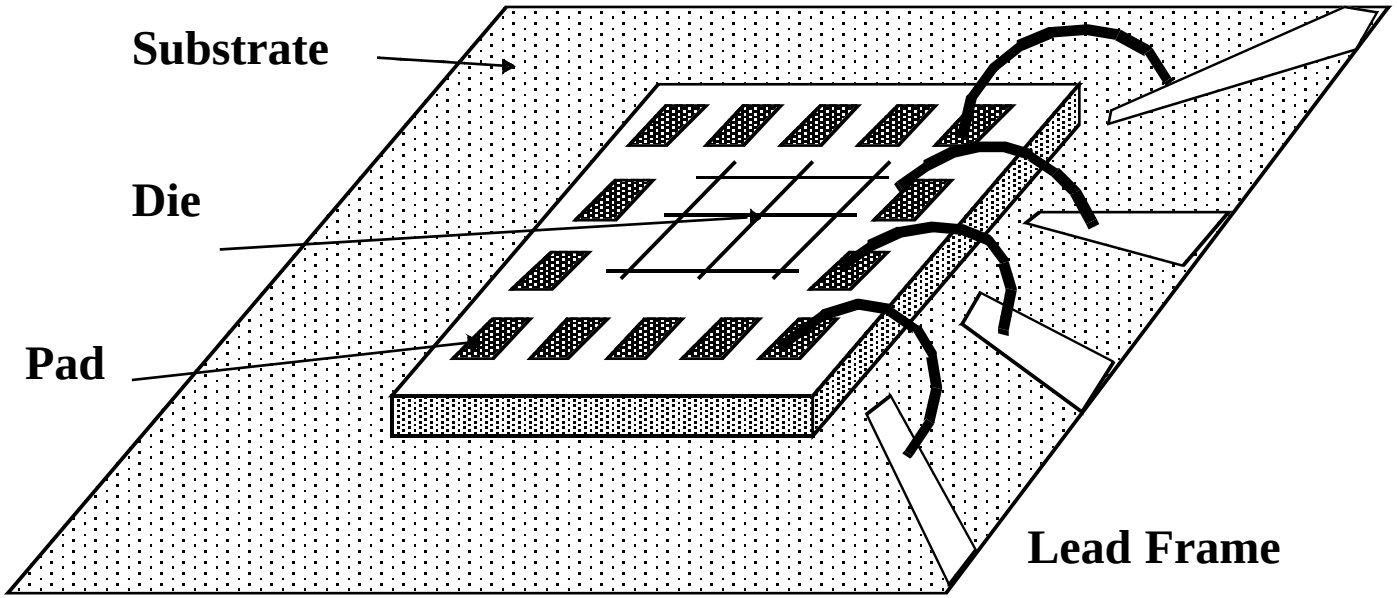
- Attained a sustained performance of **70.72 Teraflops**
  - eclipsing 3 year old top mark of **35.86 Teraflops** - Japanese Earth Simulator
  - recent mark of **42.7 Teraflops** at the NASA's Ames research center

Chip to Package Connections

1) Wire bonding
   - die attached
   - gold or aluminum wires
   - one at a time
   - not entirely repeatable
   - Electrical characteristics:
     - R: low
     - C: low
     - L: ~1 nH/mm

Bonding Techniques

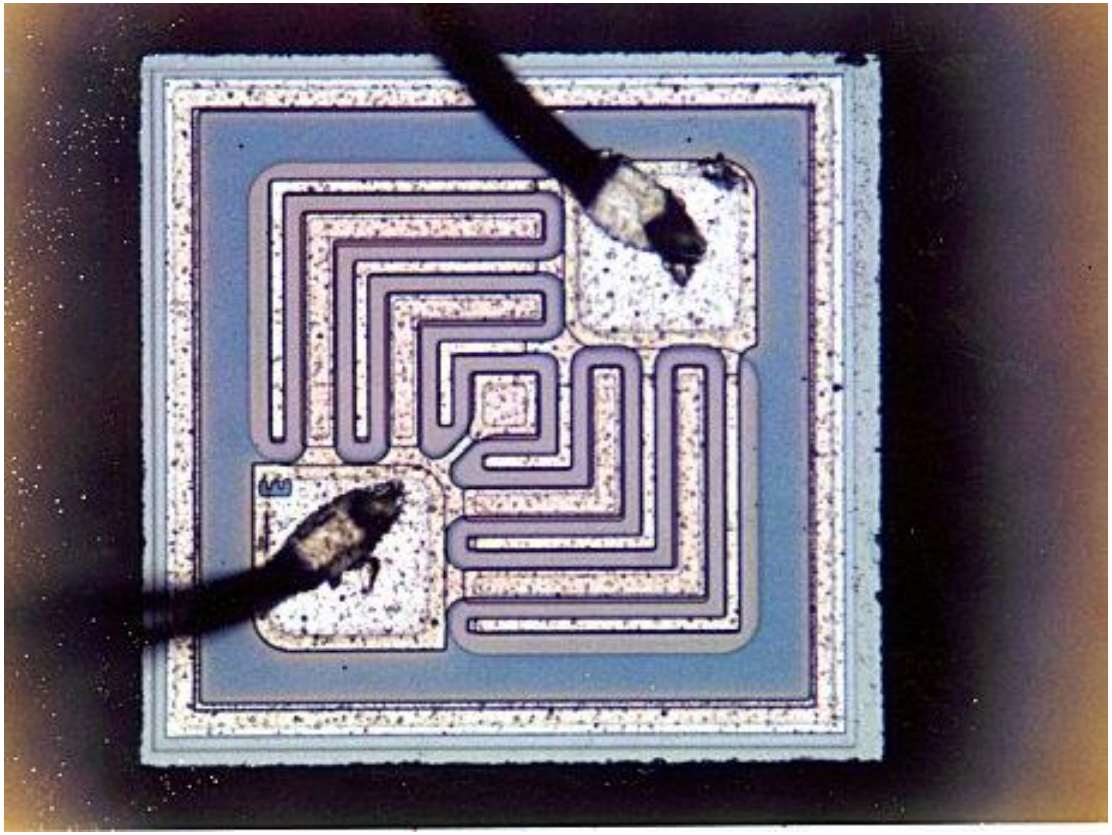
Wire Bonding



Source: Digital Integrated Circuits, 2nd ©

Wire Bonds

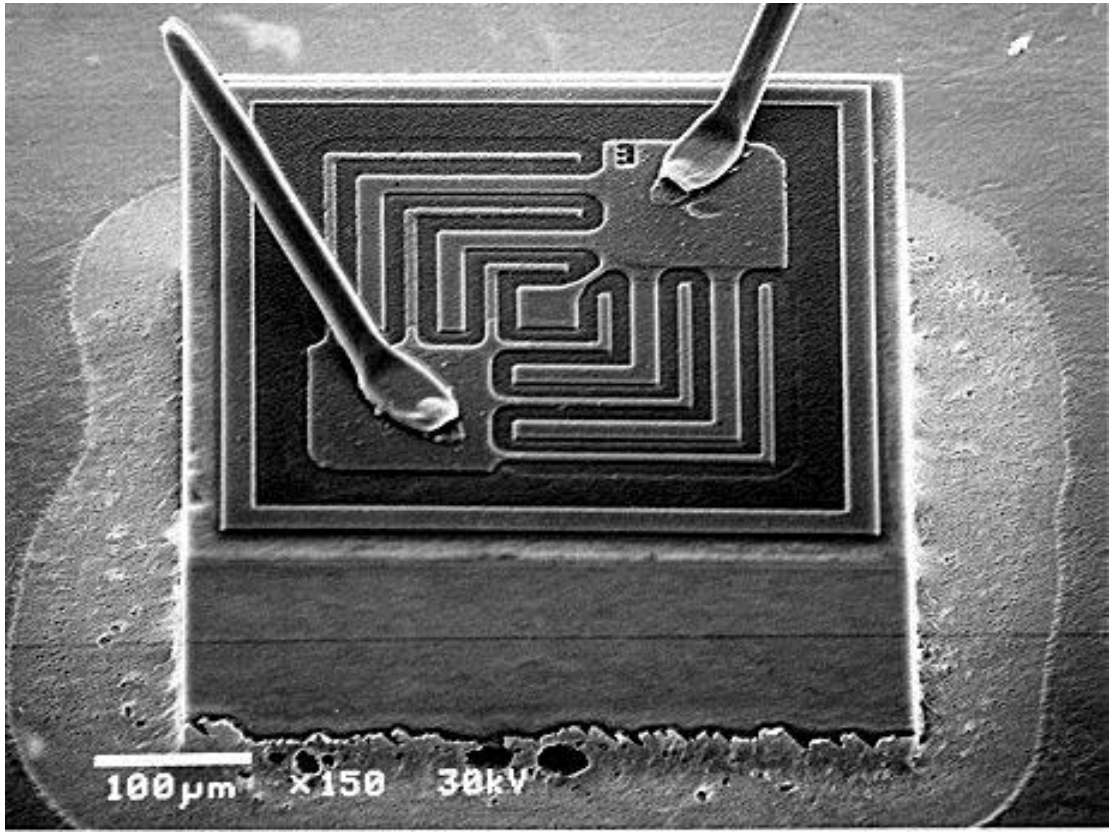
- Optical microscope view of bond wires for a two-pad package



Source: Assurance Technology

Wire Bonds

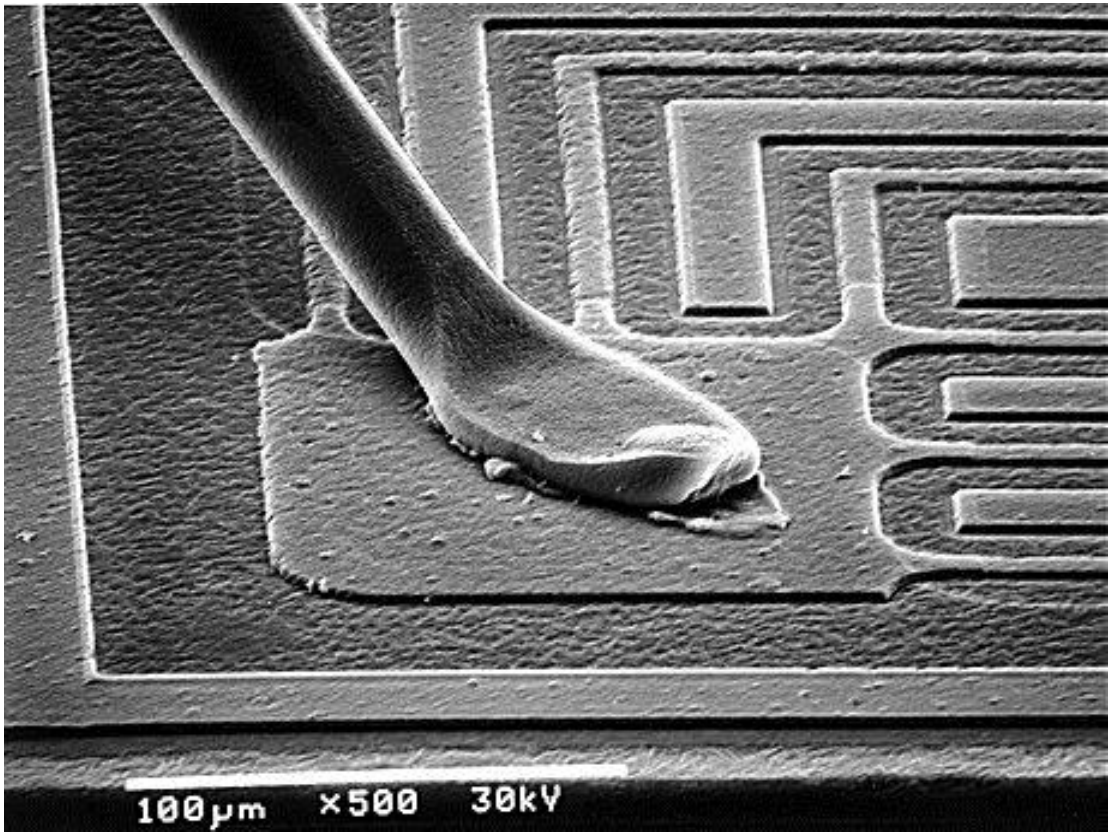
- SEM view of bond wires for a two-pad package



Source: Assurance Technology

Wire Bonds

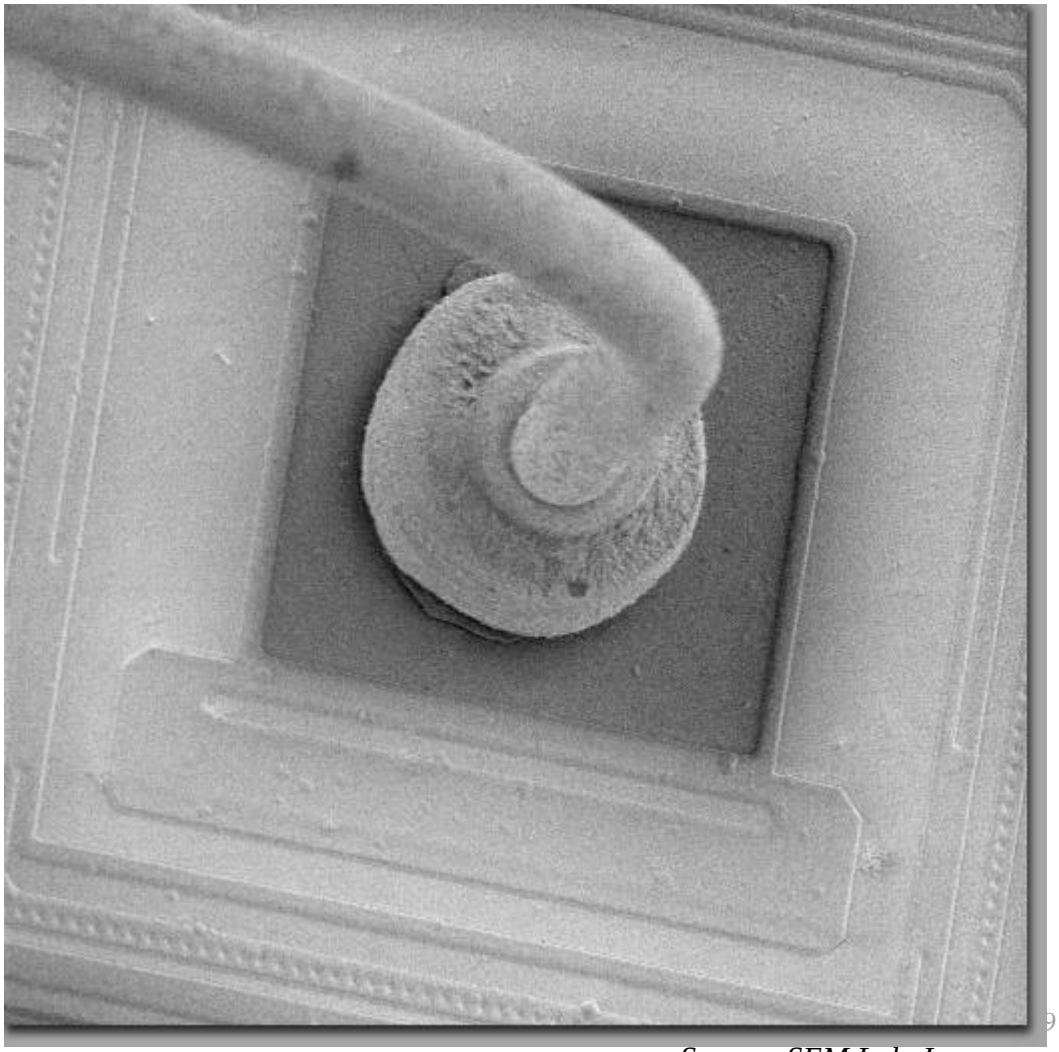
- SEM view of a single bond wire attachment



Source: Assurance Technology

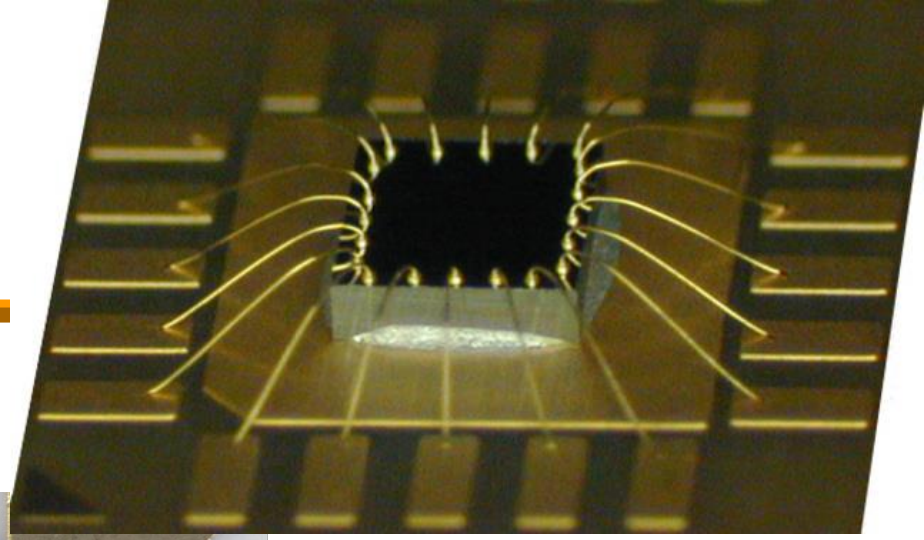
Wire Bonds

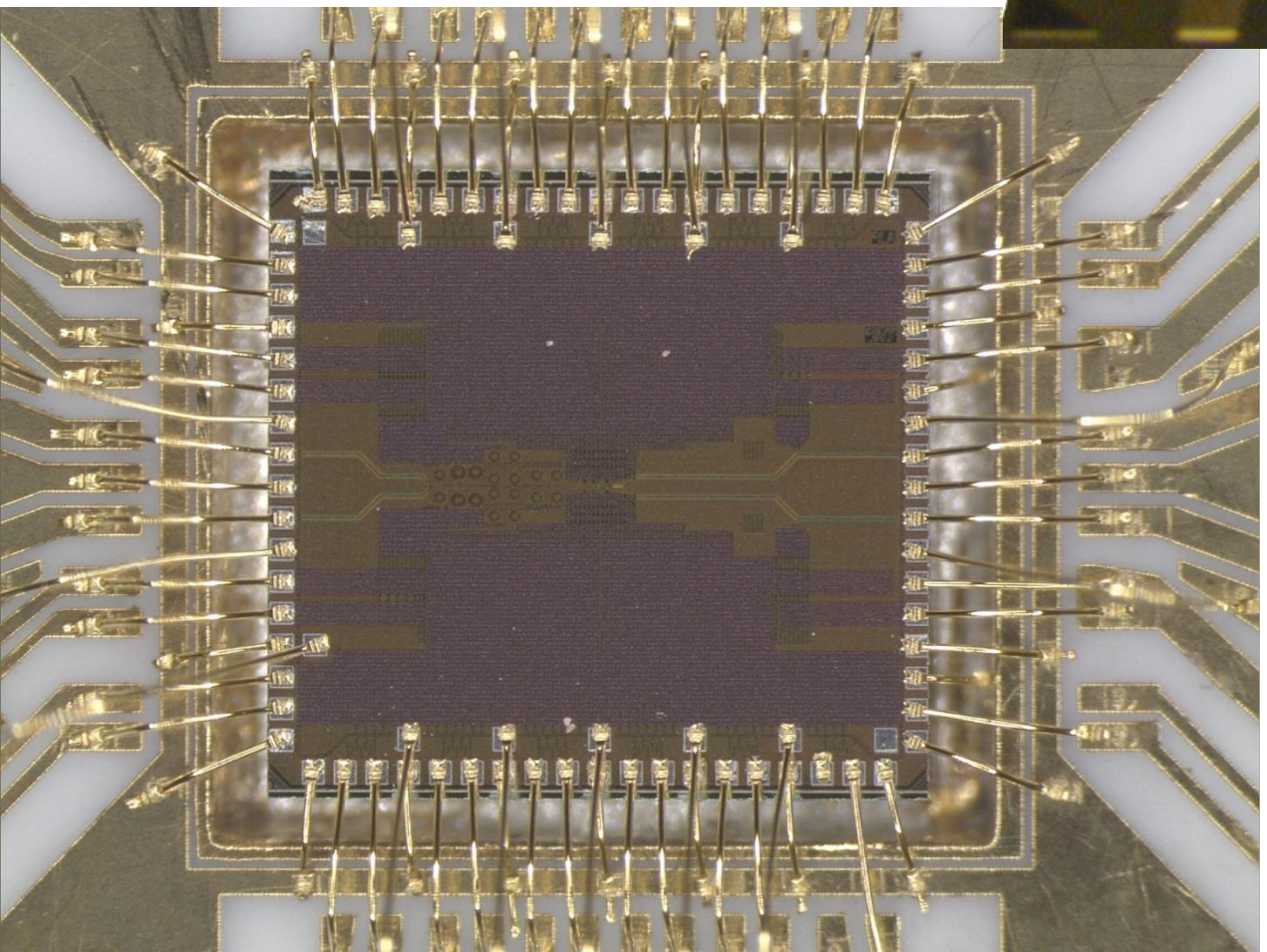
- Gold wire bond on aluminum die pad



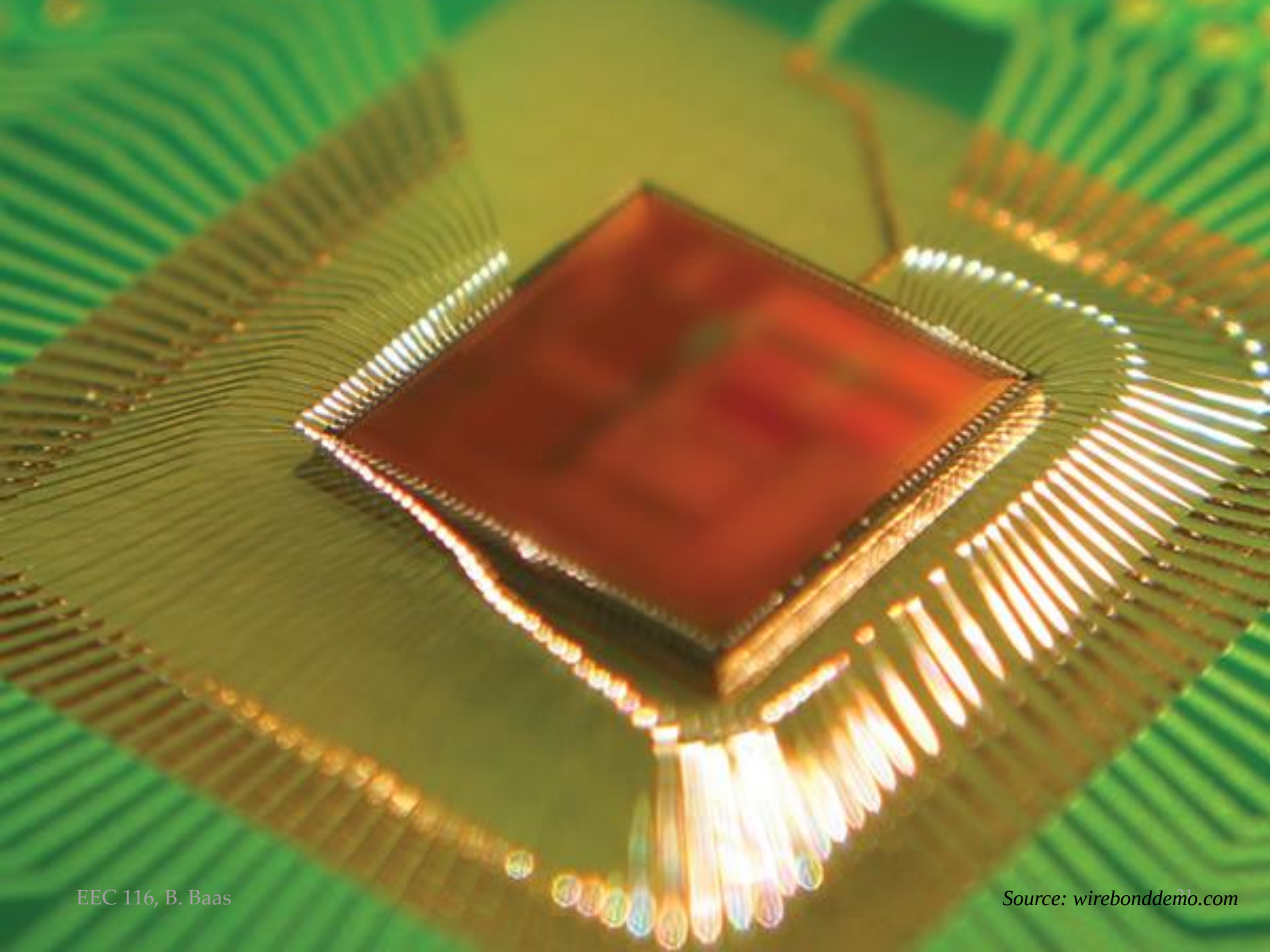
Source: SEM Lab, Inc.

Wire Bonds, Typical



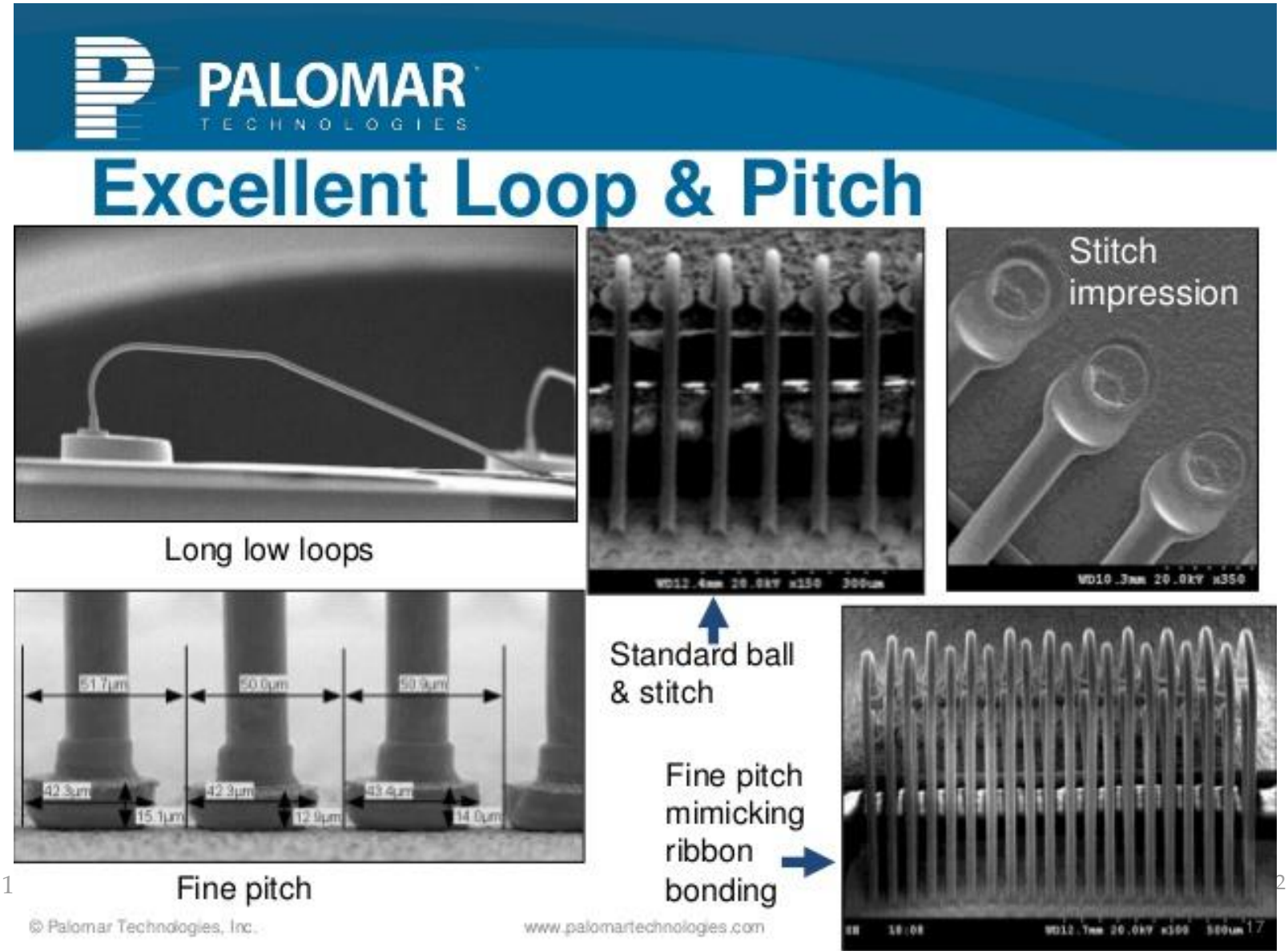


Sources: cube.cz, hwmicrolab.de



Source: wirebonddemo.com

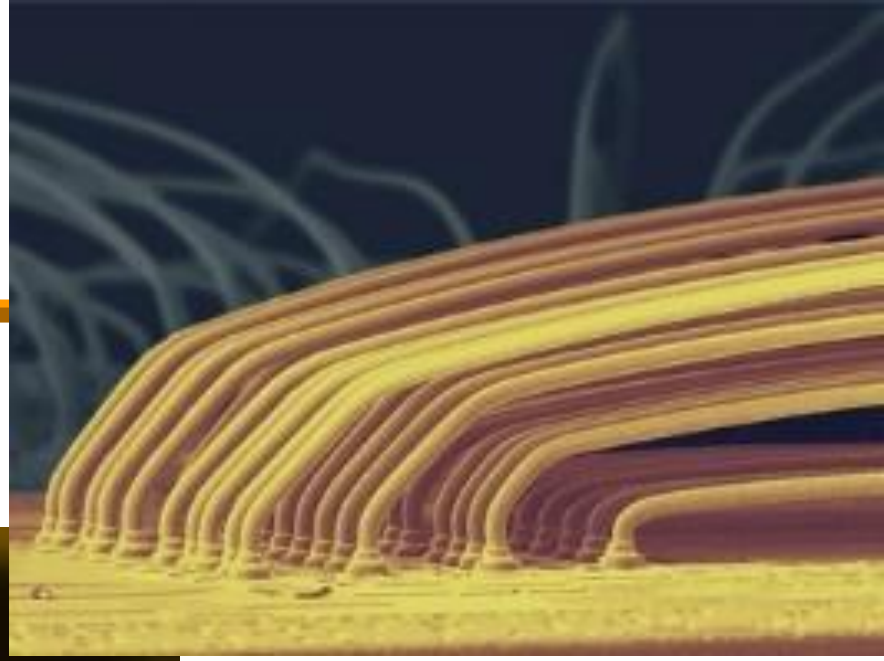
Wire Bonds

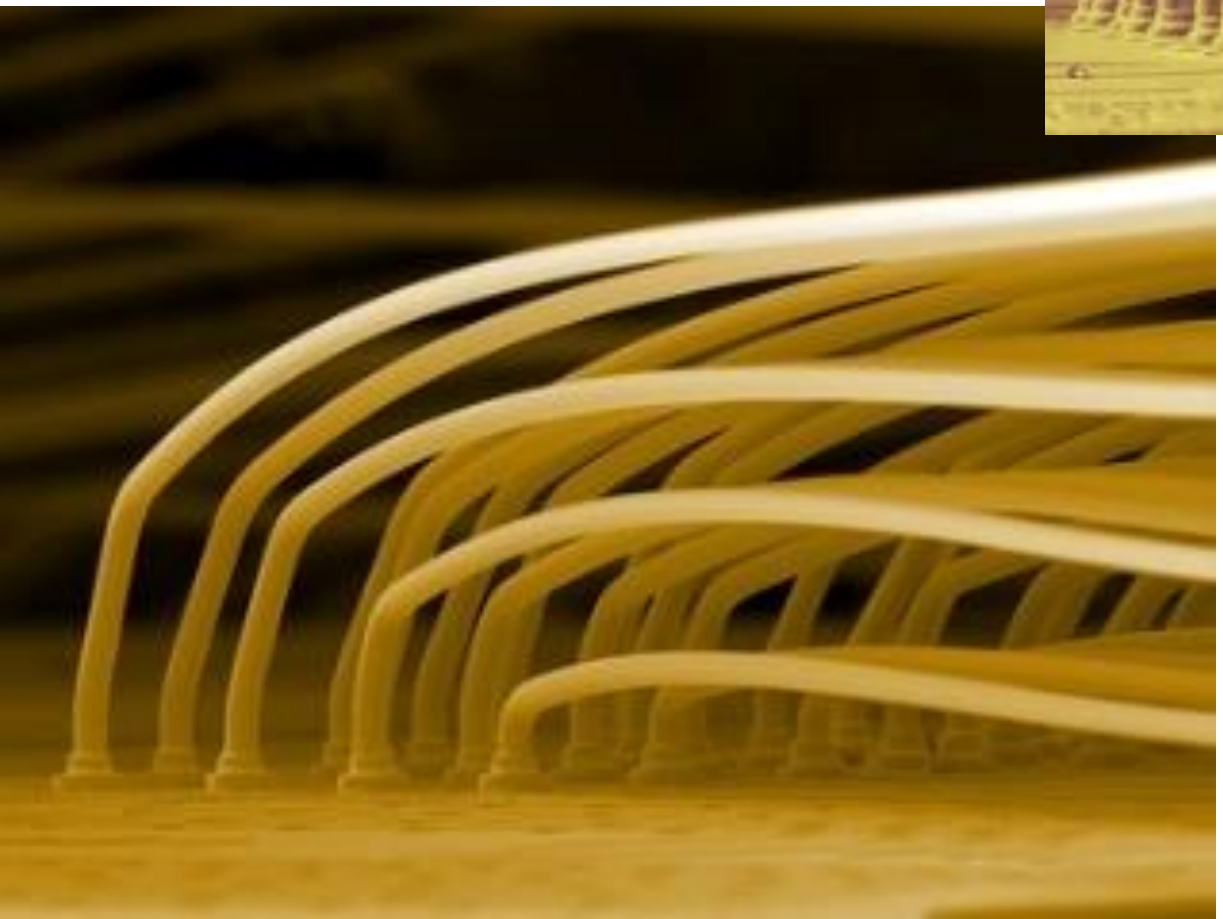


50 um pitch!

Wire Bonds

- Advanced multiple layers of wires





Sources: kns.com

Wire Bonding Machines

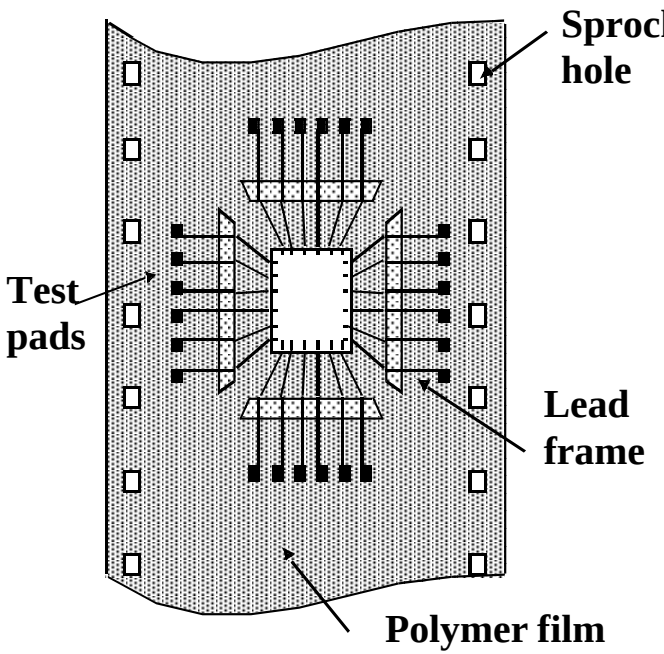
- Manual wire bonders are often used for research chips (e.g., a few chips with less than a few hundred wires)
- A computer-controlled wire bonding machine is used for volume manufacturing

Sources: barryind.com, TWI, Ltd.

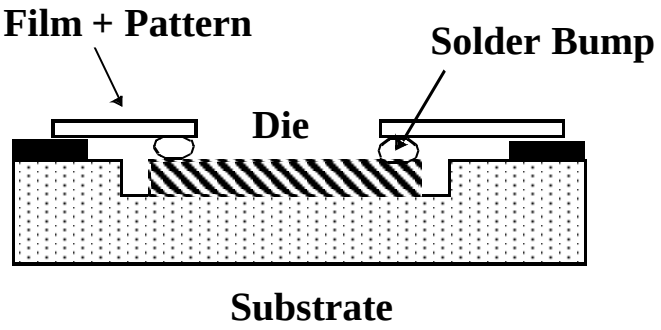
Chip to Package Connections

2) Tape automated bonding (TAB)
   - Die attached to metal lead frame printed on polymer film using solder bumps
   - Tape then connected to package
   - Fast and parallel operation
   - Lower electrical parasitics (R, L, C)

Tape-Automated Bonding (TAB)



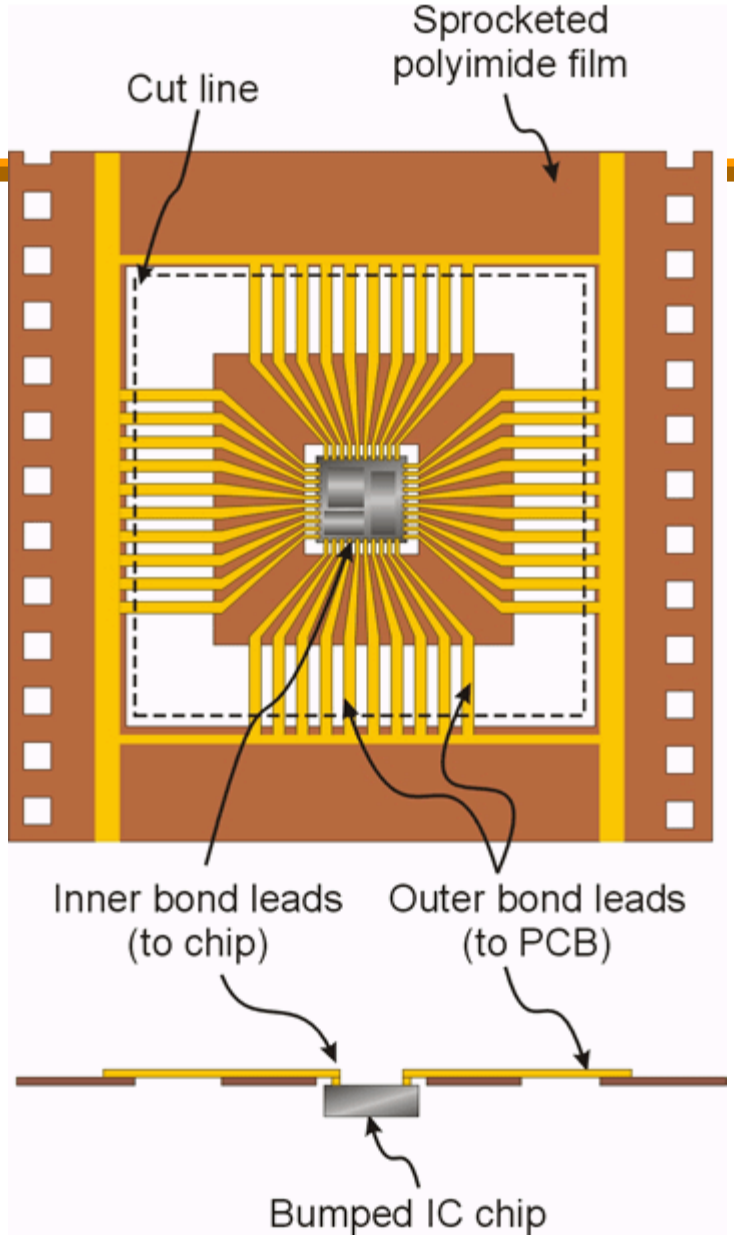
(a) Polymer Tape with imprinted wiring pattern.



(b) Die attachment using solder bumps.

Source: Digital Integrated Circuits, 2nd ©

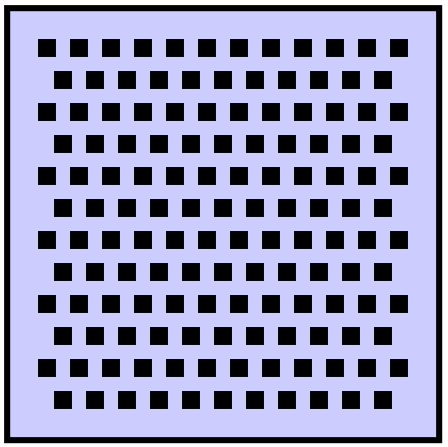
Tape-Automated Bonding (TAB)



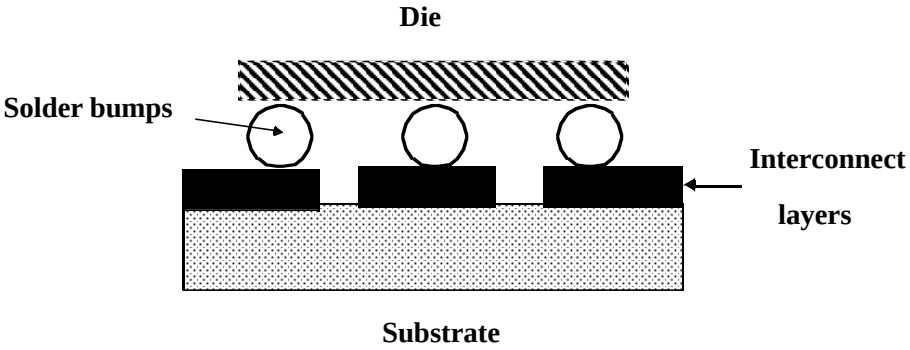
Source: Computer Desktop Encyclopedia

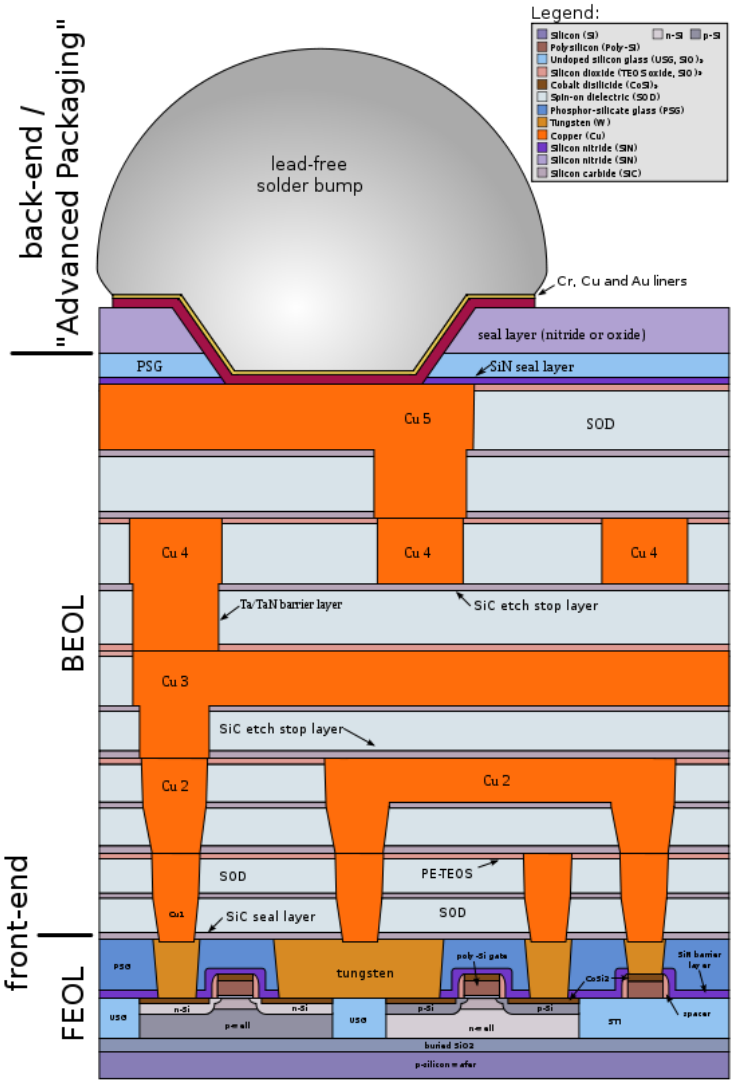
Chip to Package Connections

3) Flip chip solder bump
   - chip placed face down in package
   - connected with solder bumps
   - very low parasitics
   - allows "area pads"
     - pads can cover chip area and are not limited to chip periphery



Flip-Chip Bonding





Digital Integrated Circuits, 2nd ©
https://en.wikipedia.org/wiki/Back_end_of_line

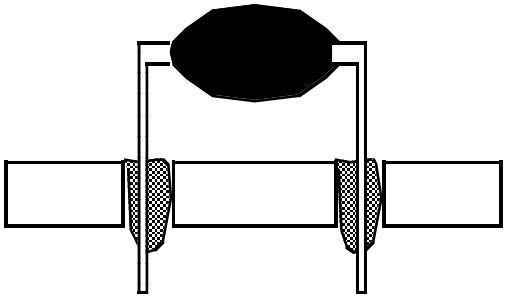
Package to Board Connections 1) Through Hole

- Classic approach
- Holes drilled and plated with copper
- Soldering
  - Chips placed inside holes
  - Bottom of board passed through a molten solder "wave"

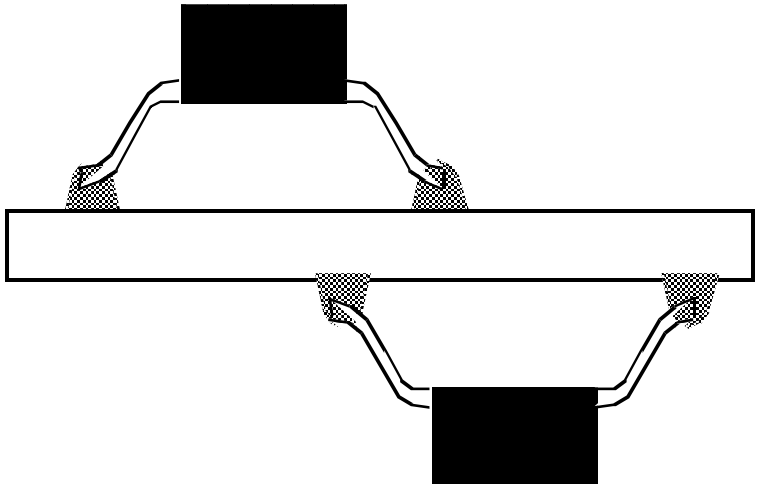
Package to Board Connections
2) Surface Mount Technology (SMT)

- More wiring room inside PC board
- Reduced space between package leads
- Chips on both sides of board
- Stronger PC board
- Soldering
  - Solder paste applied
  - Heat supplied by intense infrared light, heated air,…

Package-to-Board Interconnect



(a) Through-Hole Mounting

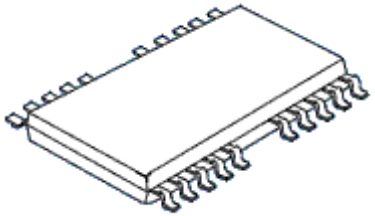


(b) Surface Mount

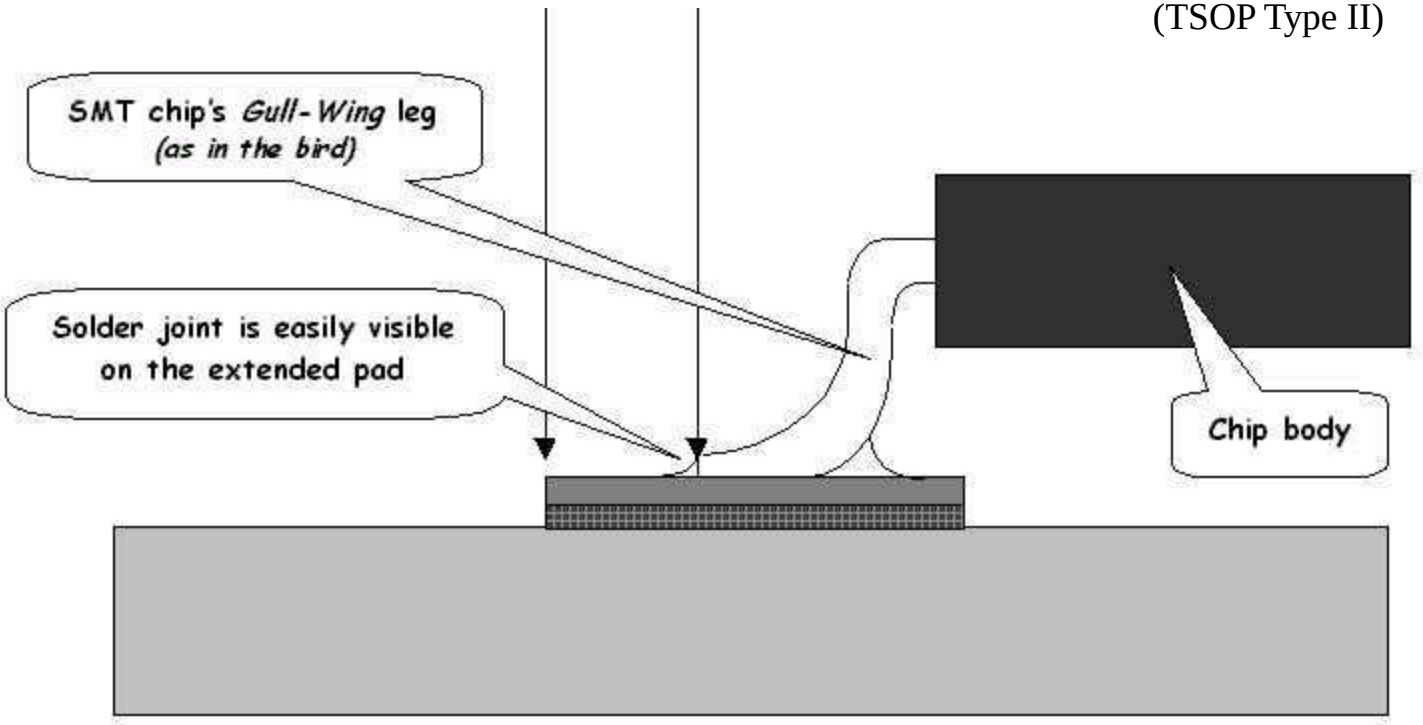
Source: Digital Integrated Circuits, 2nd ©

SMT Leads

a) *Gull-wing* SMT package leads
   - Soldering issues



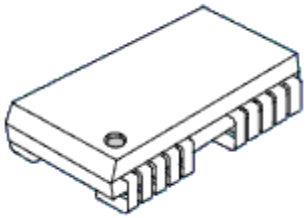
Ex: Thin Small Outline Package Type II (TSOP Type II)



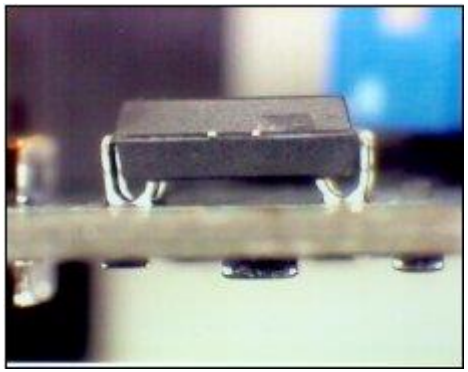
http://www.twyman.org.uk/PCB-Techniques/

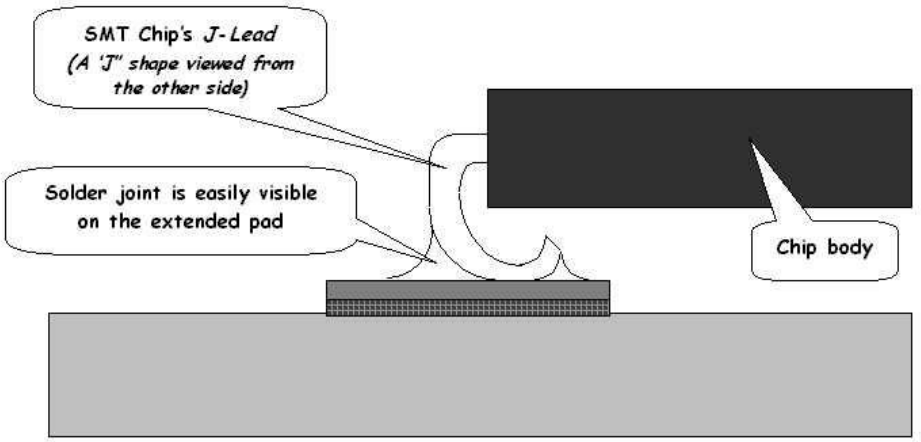
SMT Leads

b) *J-Lead* SMT package leads
- Many package types available
- Less board space than gull wing



Ex: Small Outline J-lead (SOJ)

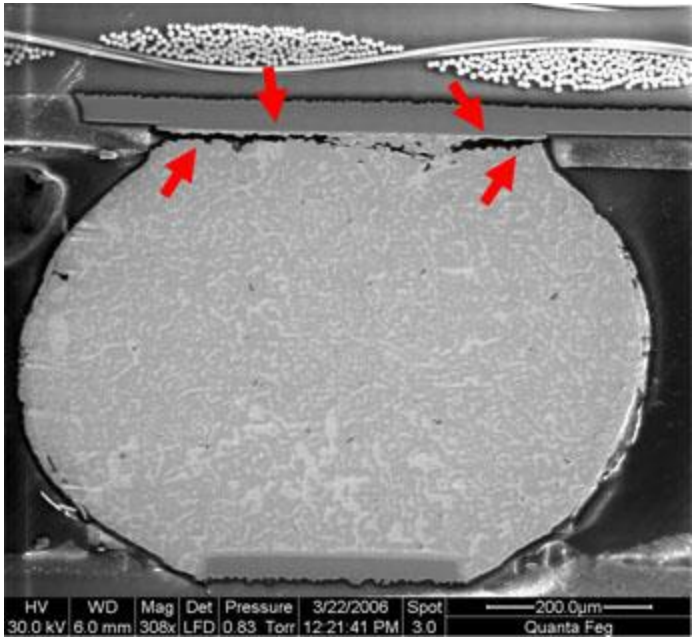




http://www.twyman.org.uk/PCB-Techniques/
http://www.ljmu.ac.uk/GERI/VERBONDS.htm

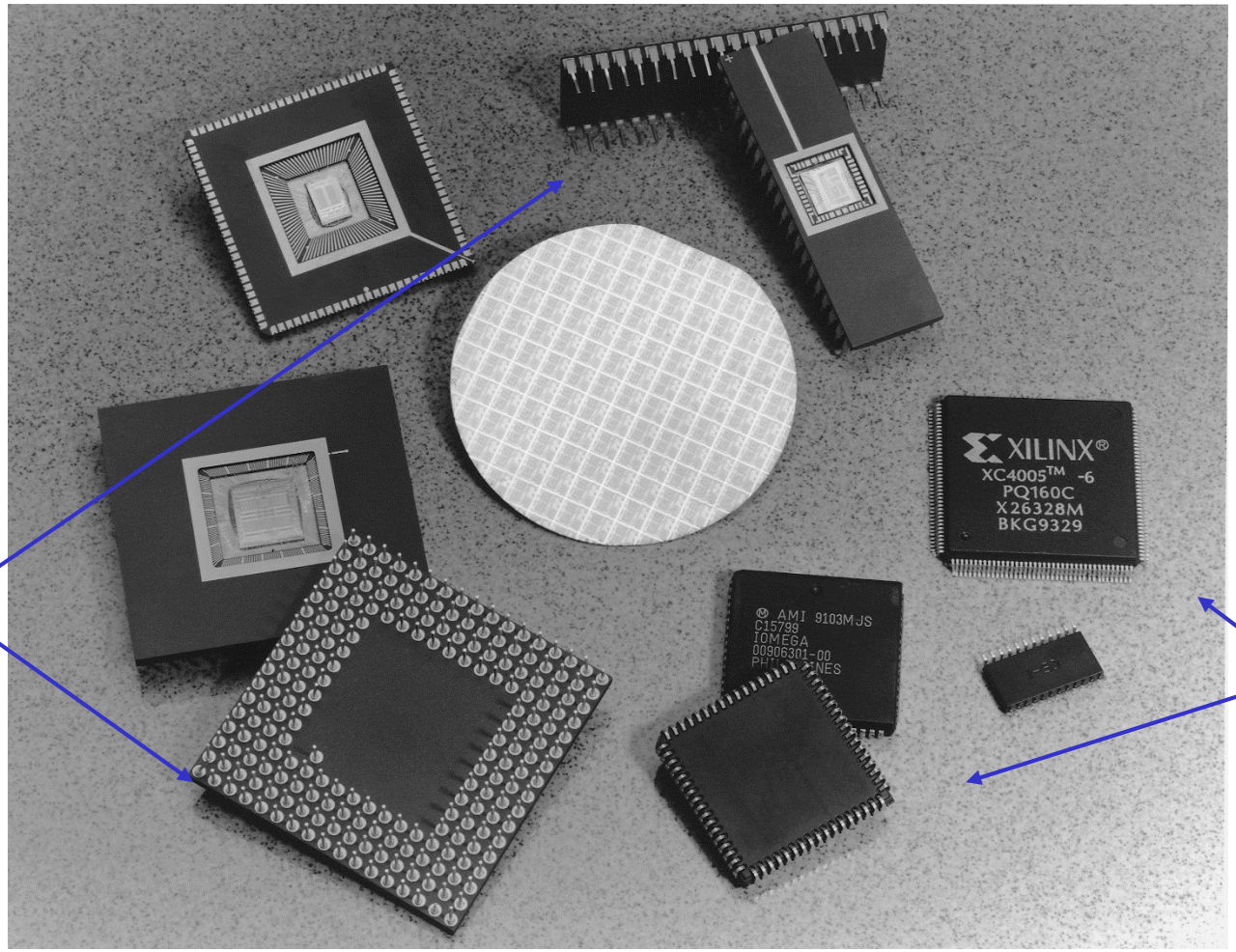
SMT "leads"

c) Solder Balls
   - Similar to flip chip but at package-to-board level
   - Very low parasitics
   - Example BGA solder ball (with highlighted crack)



http://www.calce.umd.edu/general/Facilities/sem.htm

Package Examples



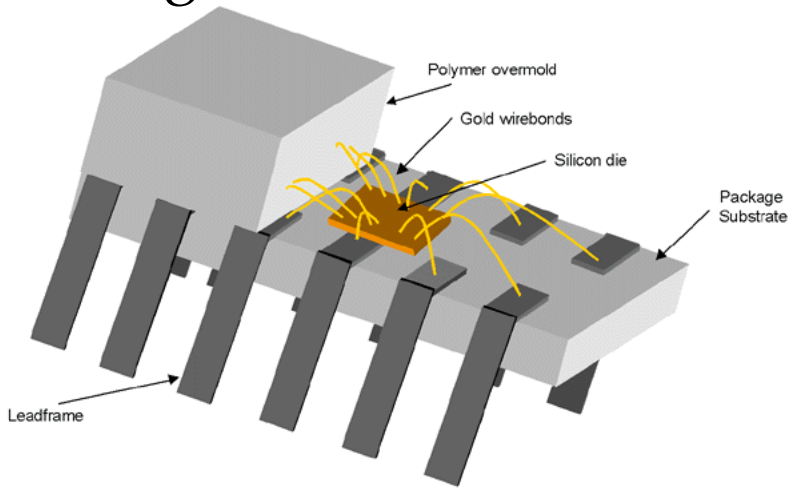
Through hole

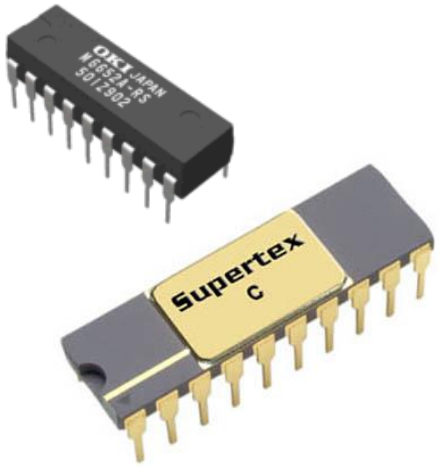
Surface mount

Source: Digital Integrated Circuits, 2nd ©

Package Types
DIP – Dual In-Line Package

- One of the oldest packaging technologies
- Low performance
- 48-64 pin packages are huge
- Cheap and abundant
- Plastic and ceramic

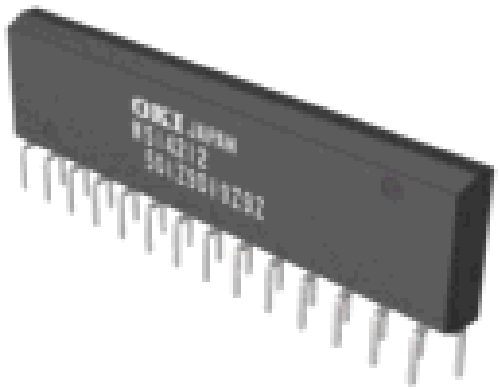




http://www.mameworld.net/gurudumps/MyStuff/packages.html
http://www.tms.org/pubs/journals/JOM/9903/Frear-9903.html
http://www.supertex.com/packaging.html
http://www.arlabs.com/help.htm
http://en.wikipedia.org/wiki/Dual_in-line_package

Package Types
ZIP – Zig-Zag In-Line Package

- Not very common



http://www.mameworld.net/gurudumps/MyStuff/packages.html

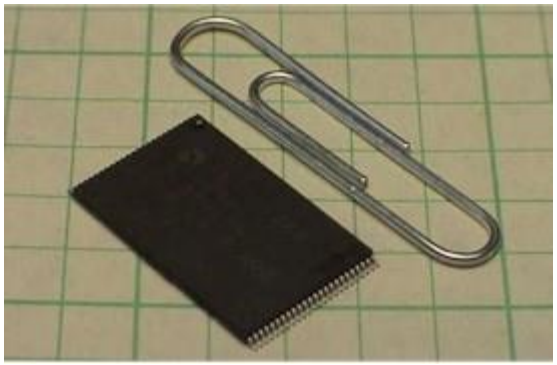
Package Types
SOP – Small Outline Package

- SOP includes a large family of packages
  - SOIC – Small Outline Integrated Circuit
  - SSOP – Shrink Small Outline Package
  - QSOP – Quarter-size Small Outline Package
  - TSSOP – Thin Shrink Small Outline Package
  - MSOP – Mini Small Outline Package

http://www.carsem.com/services/package.php
http://www.mameworld.net/gurudumps/MyStuff/packages.html

Package Types
TSOP – Thin Small Outline Package

- One of the smallest packages available
- Type I – leads on short sides

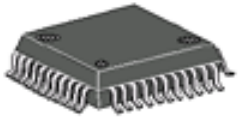


- Type II – leads on long sides

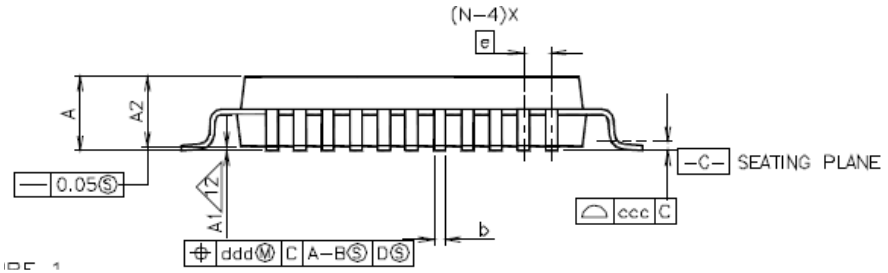
http://www.mameworld.net/gurudumps/MyStuff/packages.html
http://www.national.com/packaging/dual.html

Package Types
QFP – Quad Flat Package

- Common in modern electronics



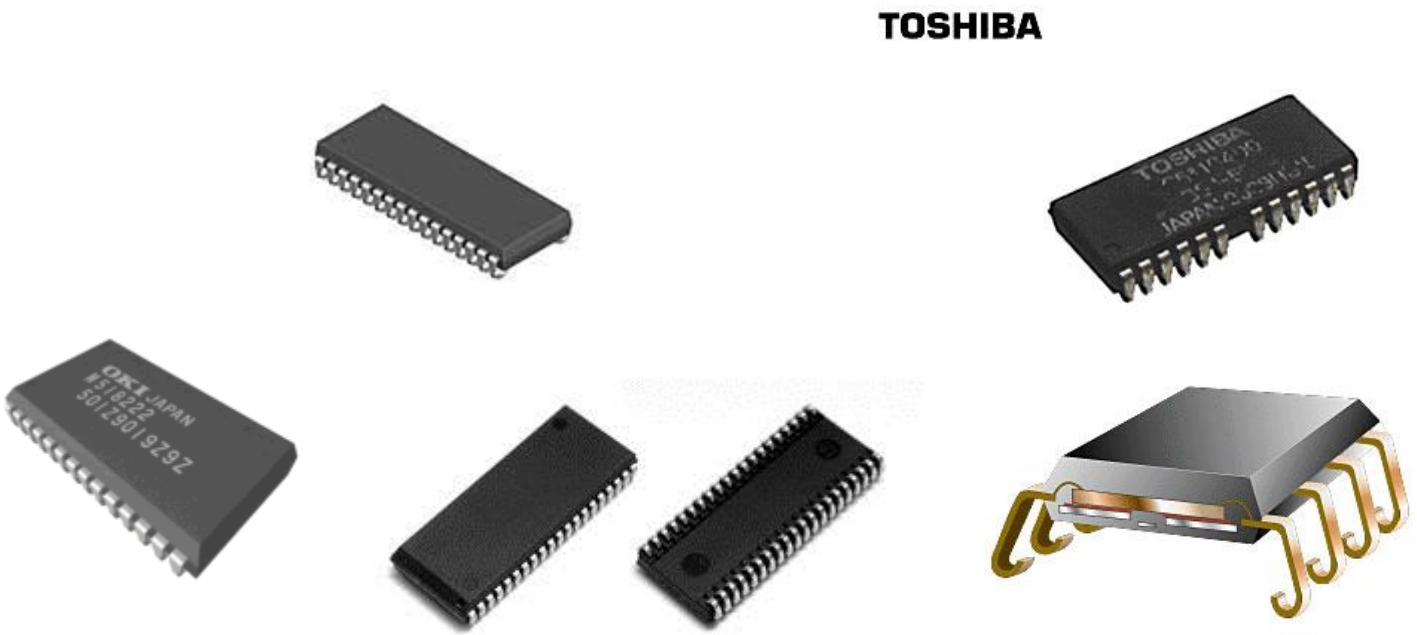
- TQFP – Thin Quad Flat Package
  - Typical thickness 1.4 mm



http://www.mameworld.net/gurudumps/MyStuff/packages.html
http://www.carsem.com/services/package.php

Package Types
SOJ – Small Outline J-lead

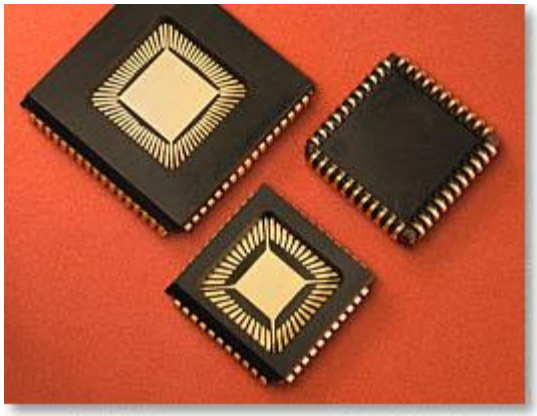
- "J" leads on two sides



http://www.mameworld.net/gurudumps/MyStuff/packages.html
http://www.national.com/packaging/dual.html
http://www.asetwn.com.tw/content/2-1-2.html
http://www.toshiba.co.jp/tech/pat/ip-disclosure/p2538717.htm

Package Types
PLCC – Plastic Leaded Chip Carrier

- Also called QFJ – Quad Flat J-lead
- Common in many products

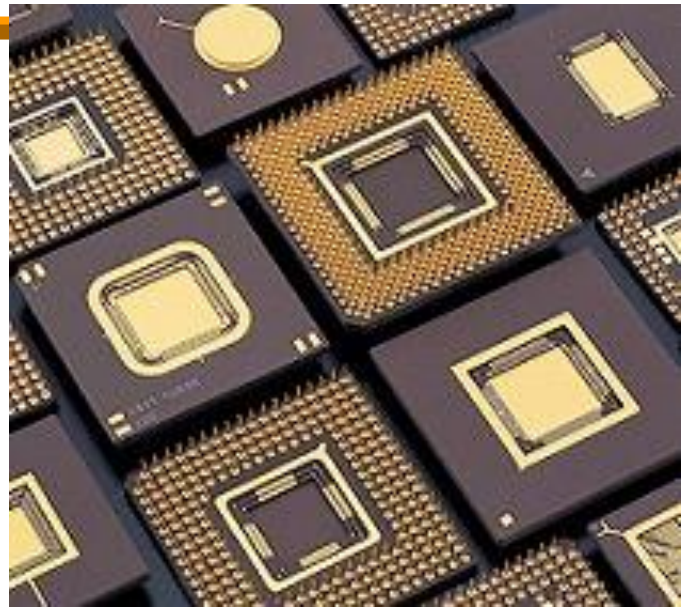


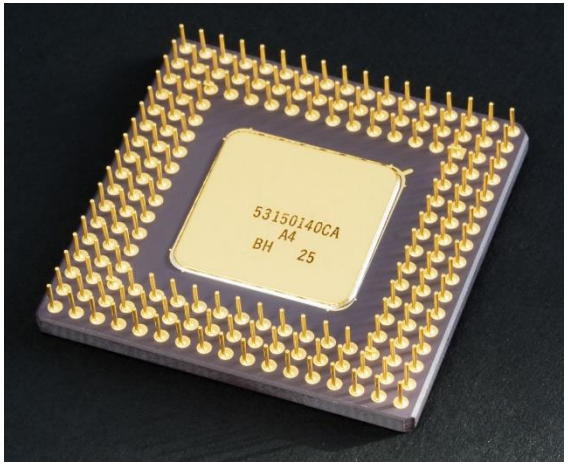
PLCC in socket

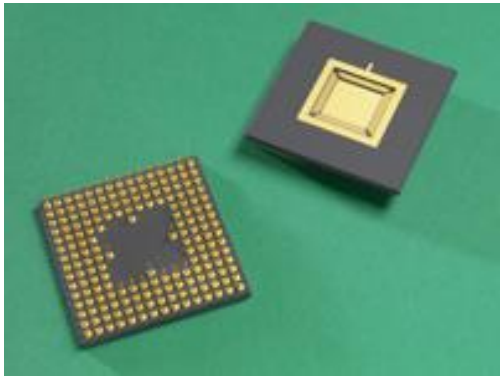
http://www.mameworld.net/gurudumps/MyStuff/packages.html
http://www.arlabs.com/help.htm
http://www.globalchipmaterials.com/visitors/products_visitors_acp_plcc.htm
http://www.statschippac.com/en-US/STATSChipPAC/IntegratedServices/Packaging/LeadFrame/plcc.htm
http://en.wikipedia.org/wiki/Plastic_leaded_chip_carrier

Package Types
PGA – Pin Grid Array Package

- Material—the main body consists of co-firing multilayer alumina ceramics, and pin terminals made of an alloy of iron, nickel, and cobalt are attached with silver-brazing to the main body.
- 400+ pins possible
- Cavity up
- Cavity down

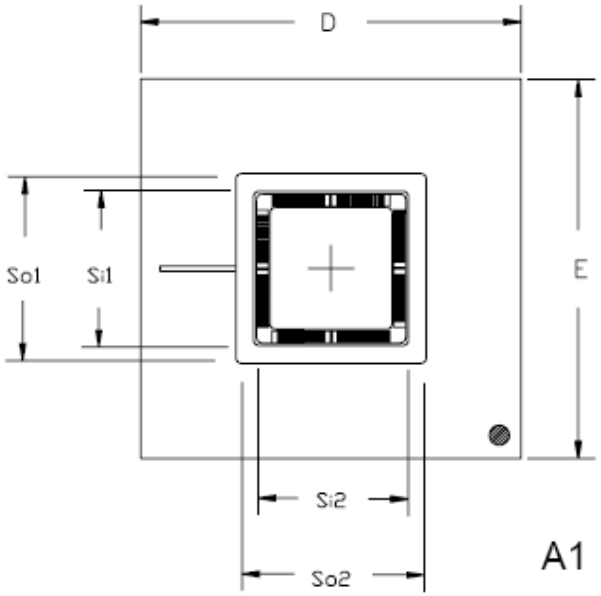


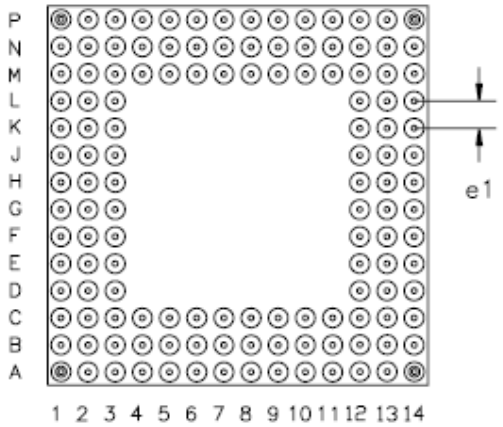




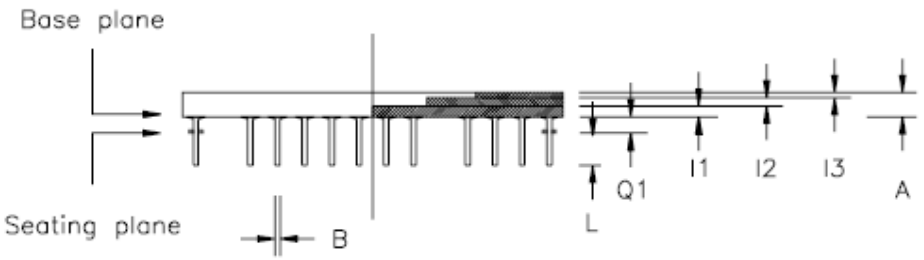
http://www.ngkntk.co.jp/english/product/semi/ic-ceramics/index.html
http://www.ntktech.com/product_detail.asp?productid=20
http://commons.wikimedia.org/wiki/Image:Intel_80486DX2_bottom.jpg

PGA – Pin Grid Array Package
Example 132-pin PGA Datasheet



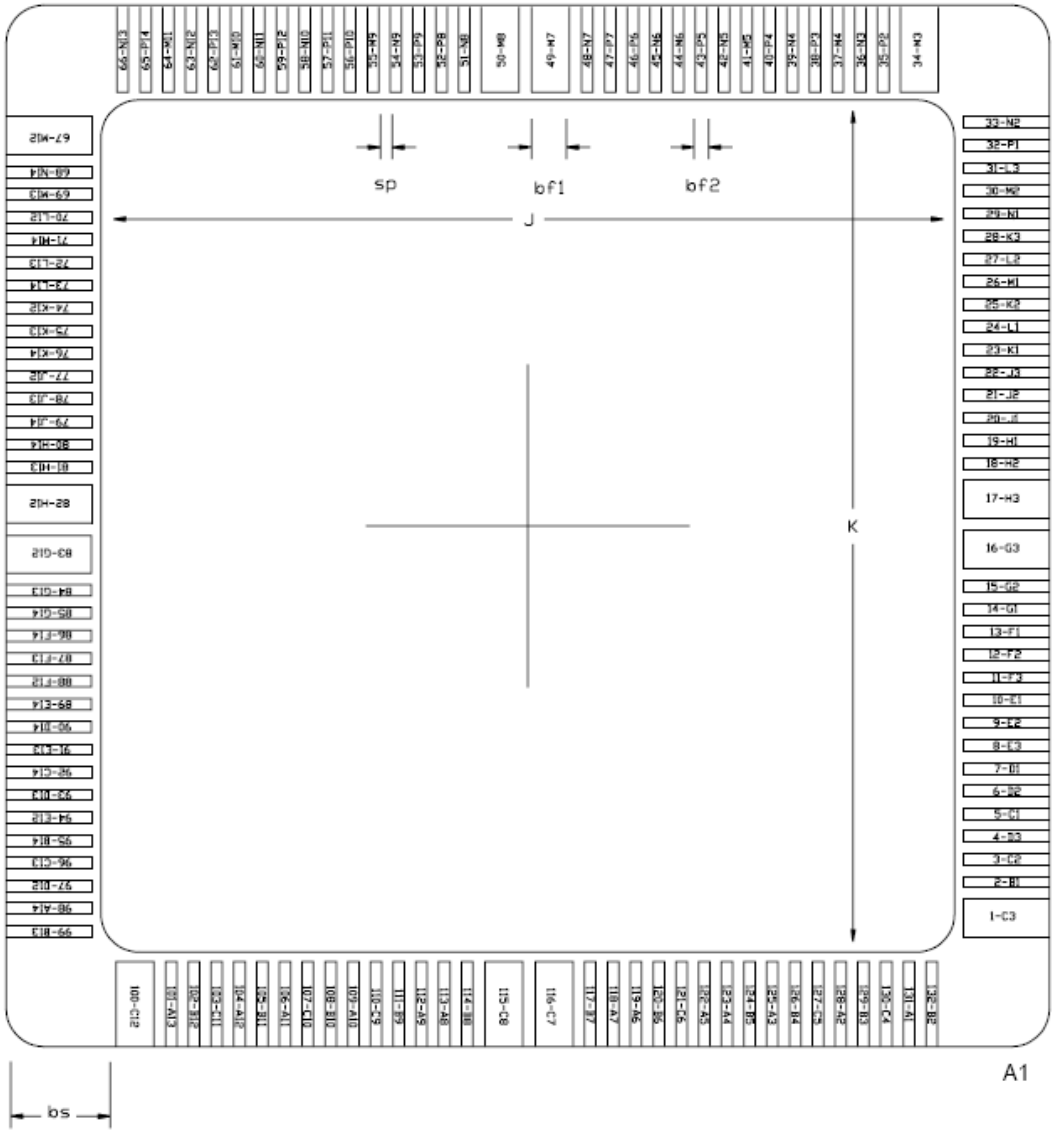


- Physical dimension drawings
- Top-side chip cavity



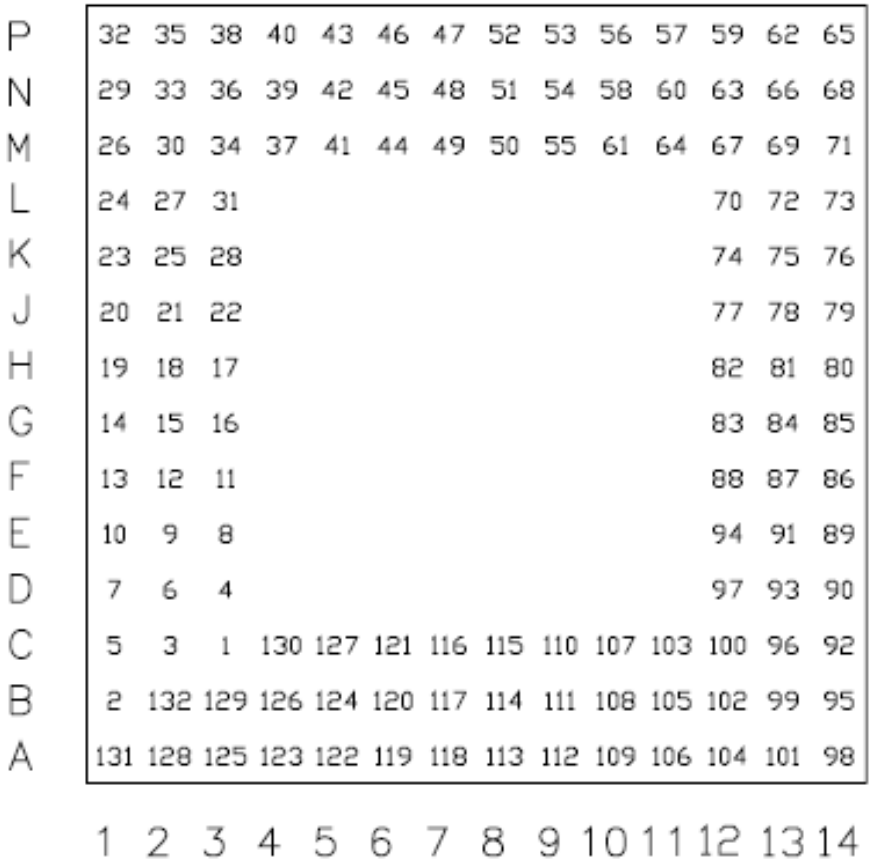
PGA – Pin Grid Array Package
Example 132-pin PGA Datasheet

- Drawing of chip cavity and 132 bond finger pads to which the bond wires are attached



PGA – Pin Grid Array Package
Example 132-pin PGA Datasheet

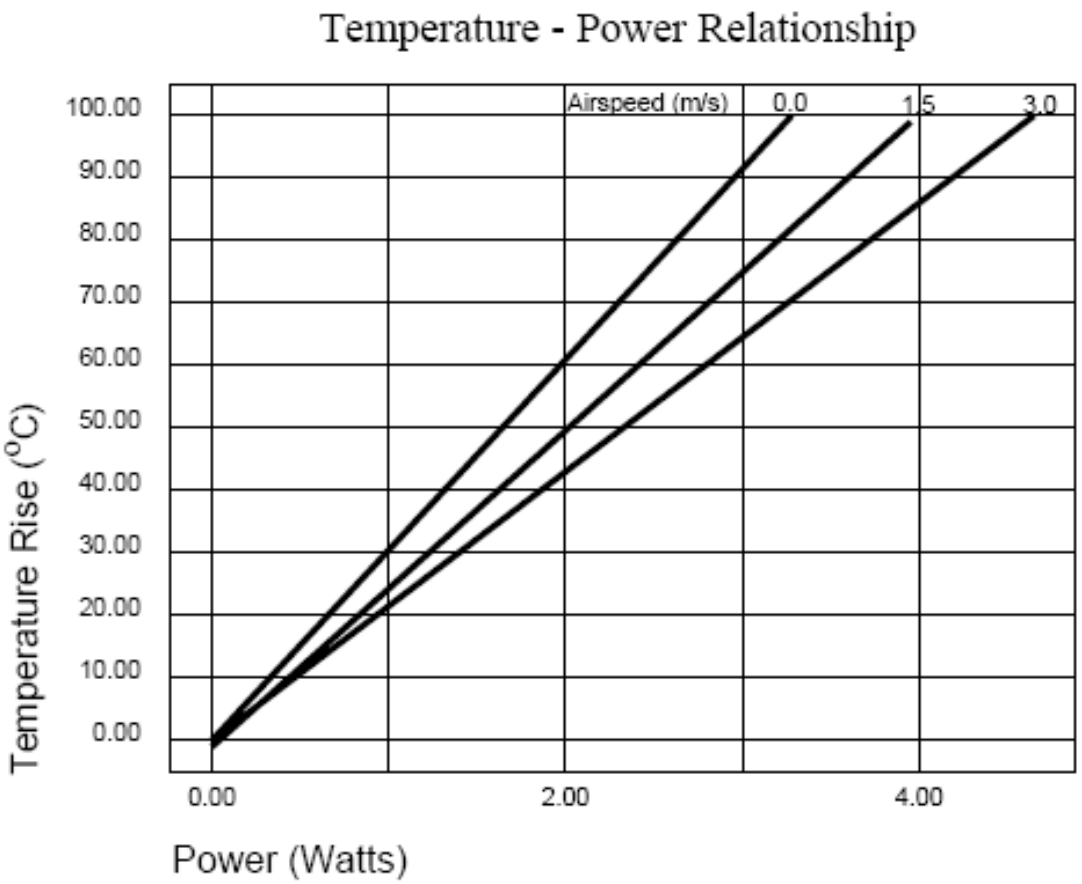
- Drawing of map showing correspondence between bond fingers and package I/O pins



Pin Side view of package

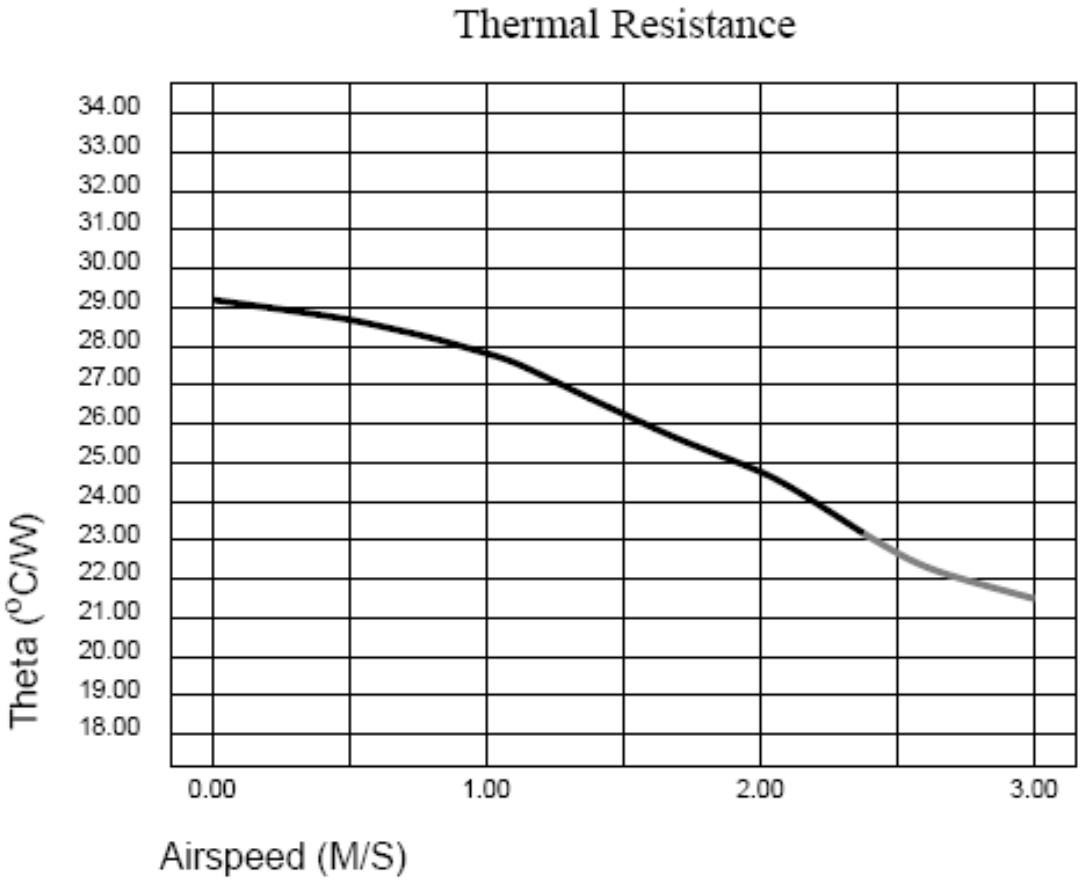
PGA – Pin Grid Array Package
Example 132-pin PGA Datasheet

- Heat dissipation capacity depends strongly on the speed of the surrounding air



PGA – Pin Grid Array Package
Example 132-pin PGA Datasheet

- More general data presentation shows thermal resistance as a function of airspeed (presumably with no heat sink)

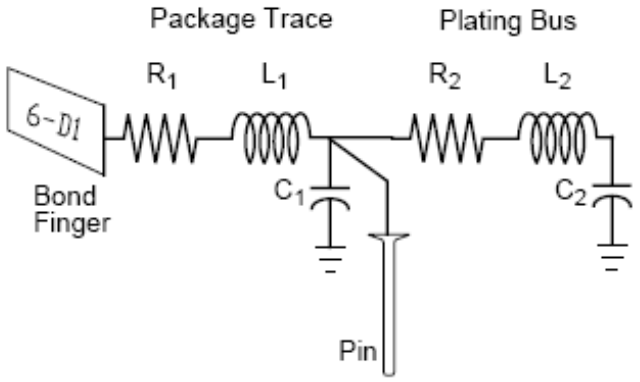


PGA – Pin Grid Array Package, Example 132-pin PGA

- Equivalent circuit and typical values
- Notice very large variance in electrical performance for different package pins
- Consider best pins for:
  - High-speed signals
  - Power and Gnd

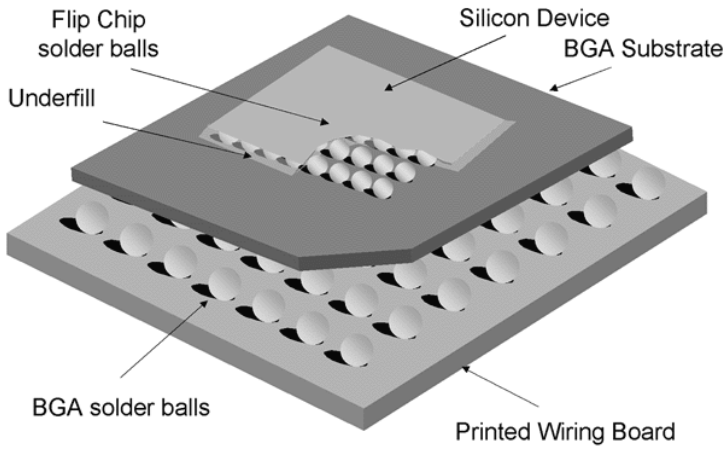
Electrical Characteristics

Bond Finger	R_1 Ω	L_1 nH	C_1 pF	R_2 Ω	L_2 nH	C_2 pF	t_{of}(ps)
11,22,44,55,77,88,110,121	0.105	3.46	1.54	0.291	4.65	1.3	72.6
8,28,41,61,74,94,107,127	0.109	3.67	1.77	0.291	4.65	1.3	79.6
16,17,49,50,82,83,115,116	0.125	4.1	1.86	0.291	4.65	1.3	86.6
4,31,37,64,70,97,103,130	0.121	4.03	1.9	0.291	4.65	1.3	86.6
1,34,67,100	0.127	4.16	1.82	0.291	4.65	1.3	86.6
15,18,48,51,81,84,114,117	0.165	5.23	2.18	0.0433	0.693	0.194	107
13,20,46,53,79,86,112,119	0.188	5.54	2.28	0.189	3.02	0.846	112
12,21,45,54,78,87,111,120	0.257	5.93	2.12	0.189	3.02	0.846	112
14,19,47,52,80,85,113,118	0.265	6.11	2.28	0.189	3.02	0.846	117
9,25,42,58,75,91,108,124	0.197	5.82	2.36	0.0433	0.693	0.194	117
3,30,36,63,69,96,102,129	0.189	6.09	2.67	0.189	3.02	0.846	127
6,27,39,60,72,93,105,126	0.243	6.43	2.55	0.189	3.02	0.846	127
10,23,43,56,76,89,109,122	0.359	6.59	2.49	0.0433	0.693	0.194	127
33,66,99,132	0.288	6.71	2.41	0.189	3.02	0.846	127
7,24,40,57,73,90,106,123	0.172	6.52	3.31	0.0433	0.693	0.194	147
5,26,38,59,71,92,104,125	0.373	8.63	3.28	0.0433	0.693	0.194	167
2,29,35,62,68,95,101,128	0.289	8.92	3.47	0.0433	0.693	0.194	176
32,65,98,131	0.288	8.77	3.8	0.0433	0.693	0.194	182

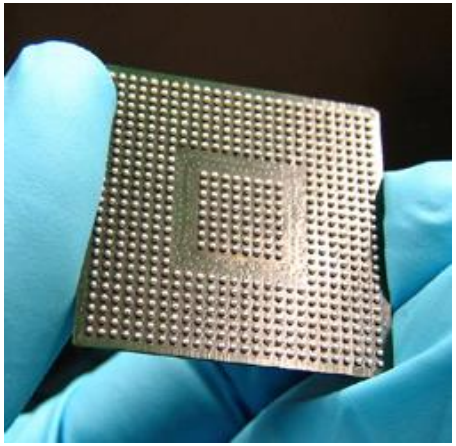


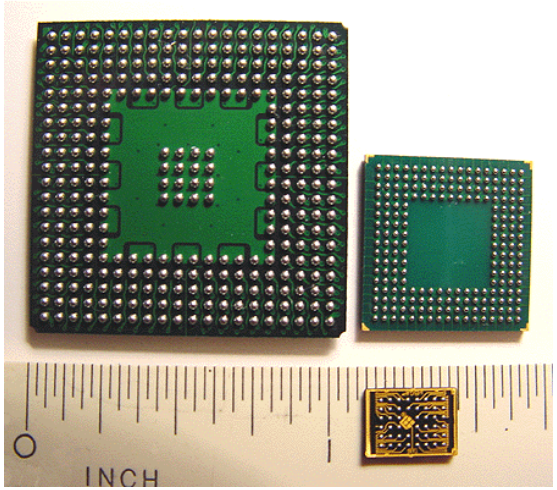
Package Types
BGA – Ball Grid Array

- Very common for high-volume high-pin-count chips
  - 200-500 I/Os is common
  - Excellent electrical characteristics
  - Good heat conduction into PC board
  - Difficult to inspect once soldered to PC board
  - Difficult to replace



BGA with Flip-Chip





http://www.mameworld.net/gurudumps/MyStuff/packages.html
http://www.pcmag.com/encyclopedia_term/0,2542,t=BGA&i=38577,00.asp
http://www.etech-web.com/bga_reballing.htm
http://www.tms.org/pubs/journals/JOM/9903/Frear-9903.html

Package Parameters

Package Type	Capacitance (pF)	Inductance (nH)
68 Pin Plastic DIP	4	35
68 Pin Ceramic DIP	7	20
256 Pin Pin Grid Array	5	15
Wire Bond	1	1
Solder Bump	0.5	0.1

Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])

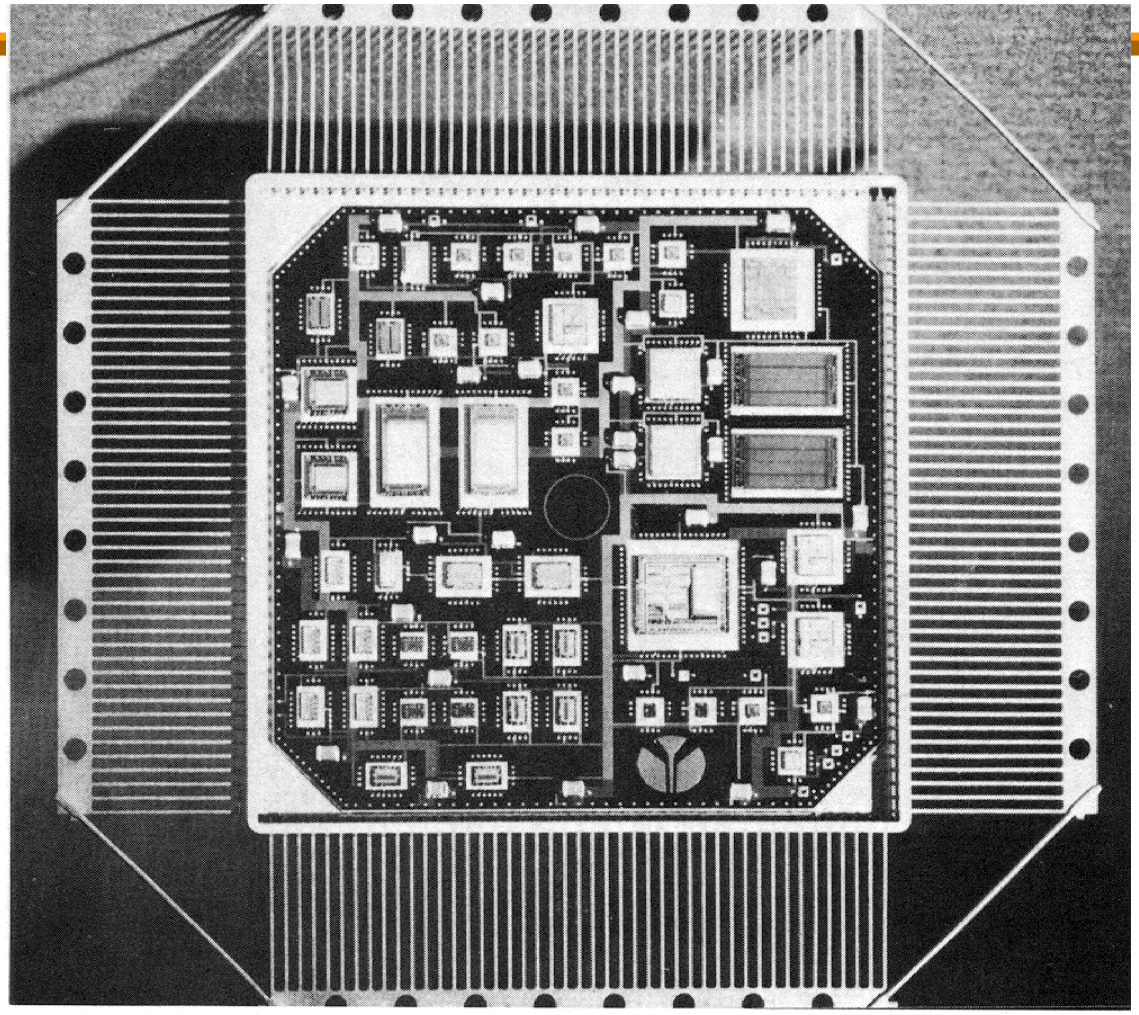
Compare with SMT values.

Source: Digital Integrated Circuits, 2nd ©

Mounting Multiple Die Directly to a Substrate

- Has been called different names at different points in time and with different substrates
  A. Multi-chip Module
     - silicon on silicon
     - many of other ceramic materials used
  B. "Chips on Board"
  C. System in Package (SiP)
- Testing is big issue
  - Repair or Scrap?
  - "known good die" are typically required but are much more difficult to test without a package

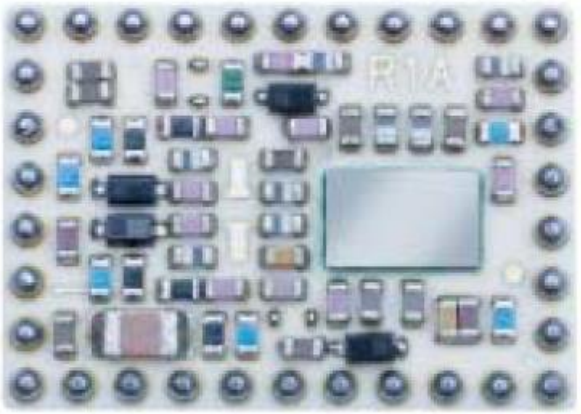
Multi-Chip Module

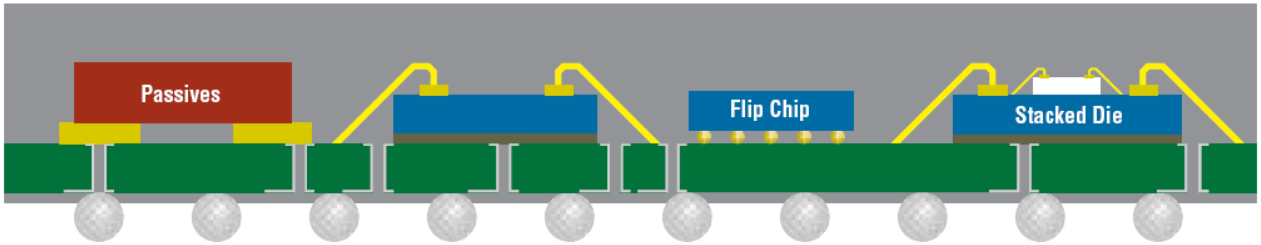


Source: Digital Integrated Circuits, 2nd ©

Package Types
SiP – System in Package

- Increasingly popular for high-volume small form factor products
- Can combine wire bonds with flip chip
- Nice solution for an application system with different types of chips and "passives" (R, L, C)

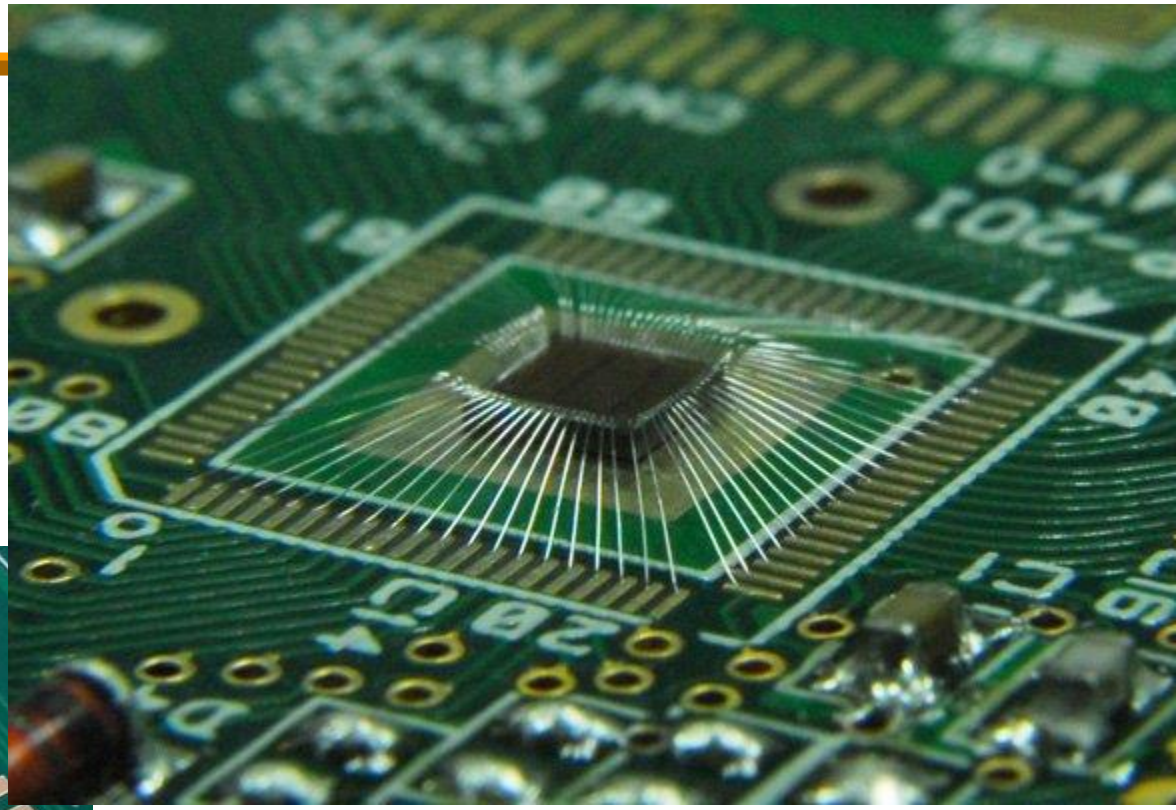


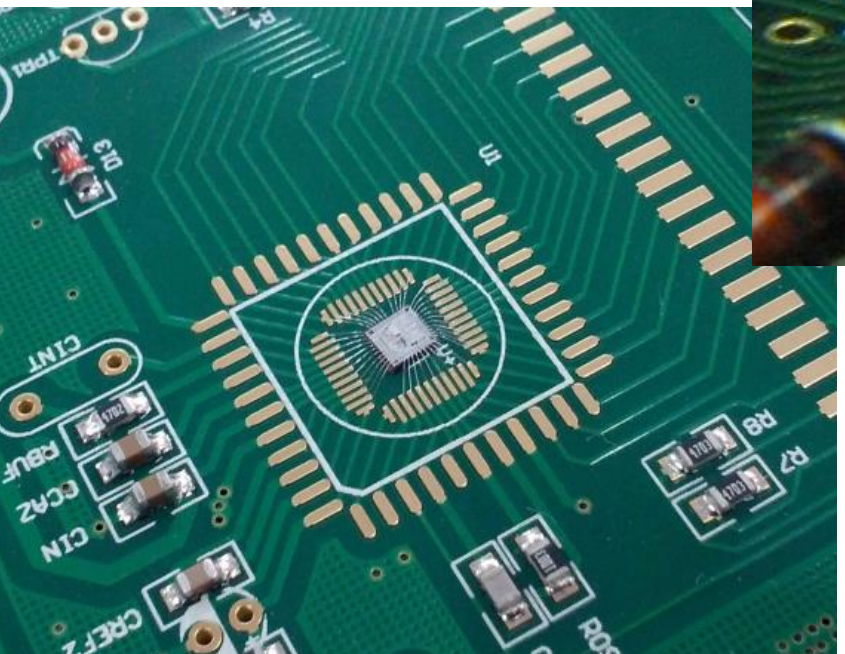


http://www.carsem.com/services/package.php

“Chips On Board”

- Not suitable for all situations
- Sometimes great for prototyping





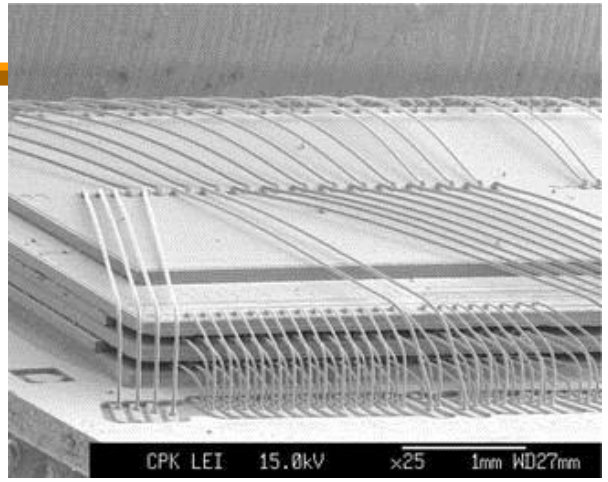
Source: pbs.twimg.com, hackadaycom,

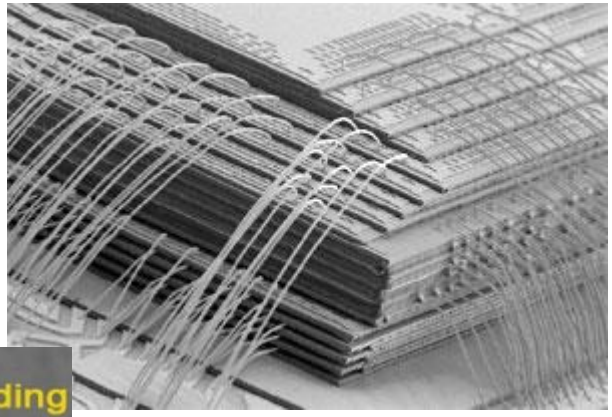
New Directions: 3D

- Vast increases in density can be achieved with 3D stacking of die
- Big issues
  - Reliability
  - Getting the heat out
  - Known good die—no chance of repair
- Package-level solutions: connect traditional die by a means such as wire bonding
- Chip-level solutions: connect stackable die by a means such as Through-Silicon-Vias (TSVs)

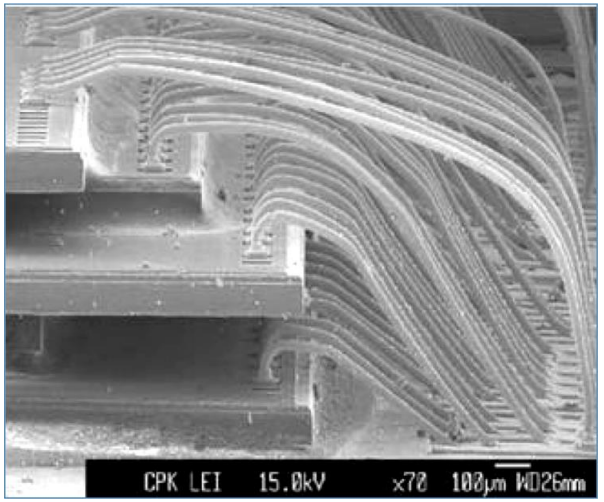
Supporting Technology for 2.5D and 3D: "Stacked Die"

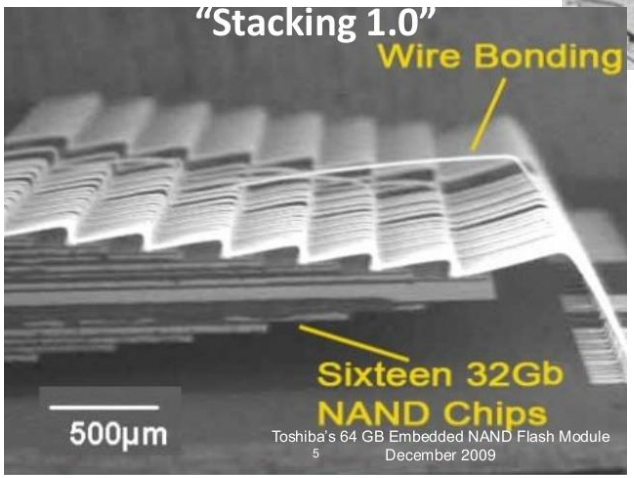
- Dense packaging methodology which places chips on top of each other
- Inter-chip interconnect can be made by a variety of means





Stack of 24 chips

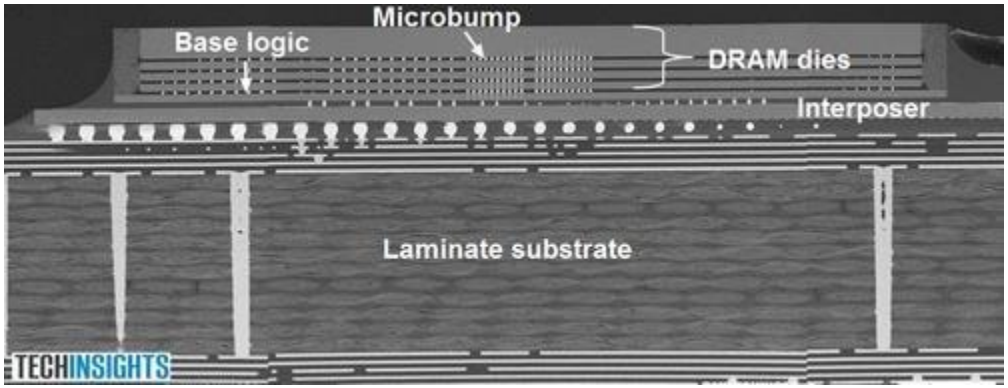


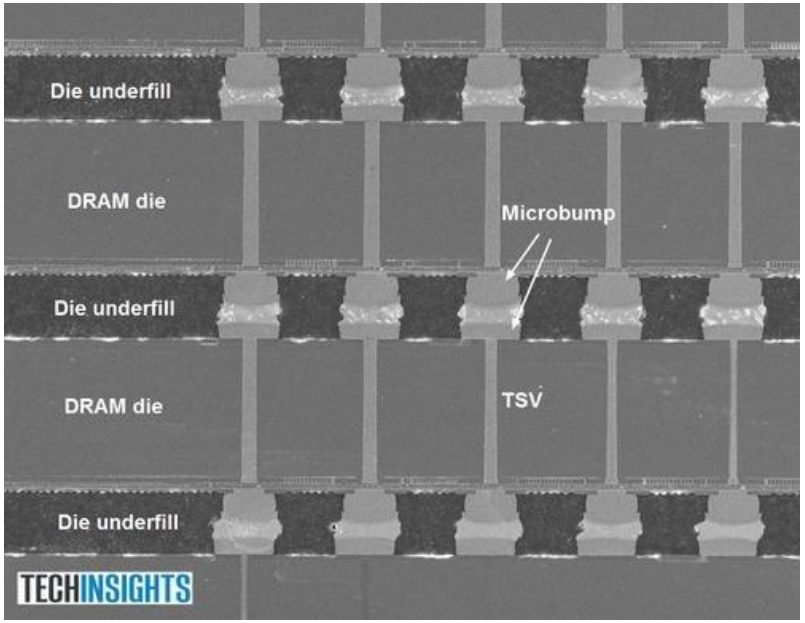


https://eprimes.wordpress.com/2011/09/21/an-overview-of-3d-integrated-circuits/
http://www.slideshare.net/iradave/deal-3-d-stacked-die-test-ira-feldman-ieee-swtw-2013
http://electroiq.com/blog/2004/08/stacked-die-packaging-technology-toolbox-step-8/
http://www.palomartechnologies.com/blog/bid/80106/Stack-Die-3D-IC-Assembly-Drivers-and-Challenges

Supporting Technology for 2.5D and 3D : "Through-Silicon Vias (TSVs)"

- Through-Silicon Vias are "vias" that connect pads on opposite sides of a chip by passing directly through the entire die
- Example: Hynix High-Bandwidth Memory (HBM) with four DRAM dies (the lower three have been thinned), a base logic die, an interposer, and a laminate substrate.



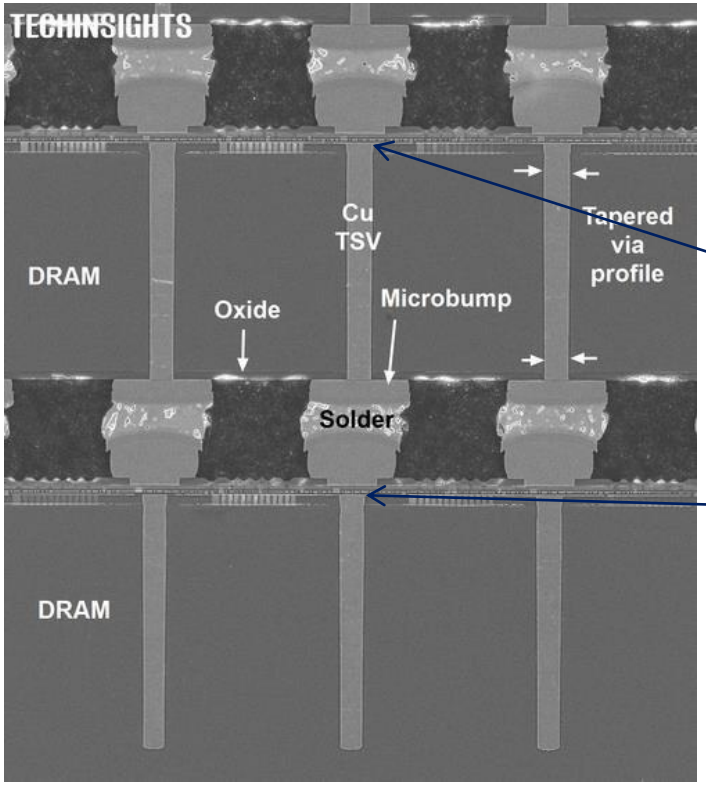


http://archive.eetasia.com/www.eetasia.com/ART_8800714409_499486_NT_874cb9d4.HTM

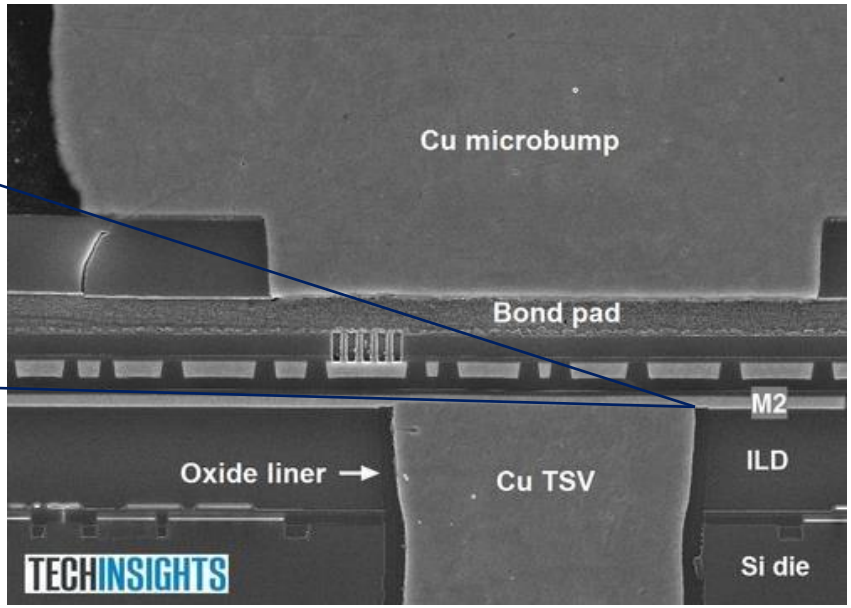
Supporting Technology for 2.5D and 3D : "Through-Silicon Vias (TSVs)"

"Hynix disclosed a via middle process for their HBM in two papers (Electronics Components & Tech. Conf. 2013 and VLSI Tech. Digest 2014). The TSV openings are formed after the tungsten contacts to the gates and source/drain regions are made, using a Bosch TSV etch. An oxide liner is then deposited along the via sidewalls, lined with a Ta-based barrier and Cu seed layers, and filled with electroplated Cu. A thermal anneal process is used as a Cu stress relief. A CMP and etch process is used to thin the backsides of the DRAM wafer and expose the Cu TSVs. The backsides of the DRAM wafers are then passivated with oxide, followed by the formation of the backside microbumps."

[http://archive.eetasia.com/www.eetasia.com/ART_8800714409_499486_NT_874cb9d4.HTM]



Images are shown inverted compared to the two previous images.



Reminder:
Cu = copper