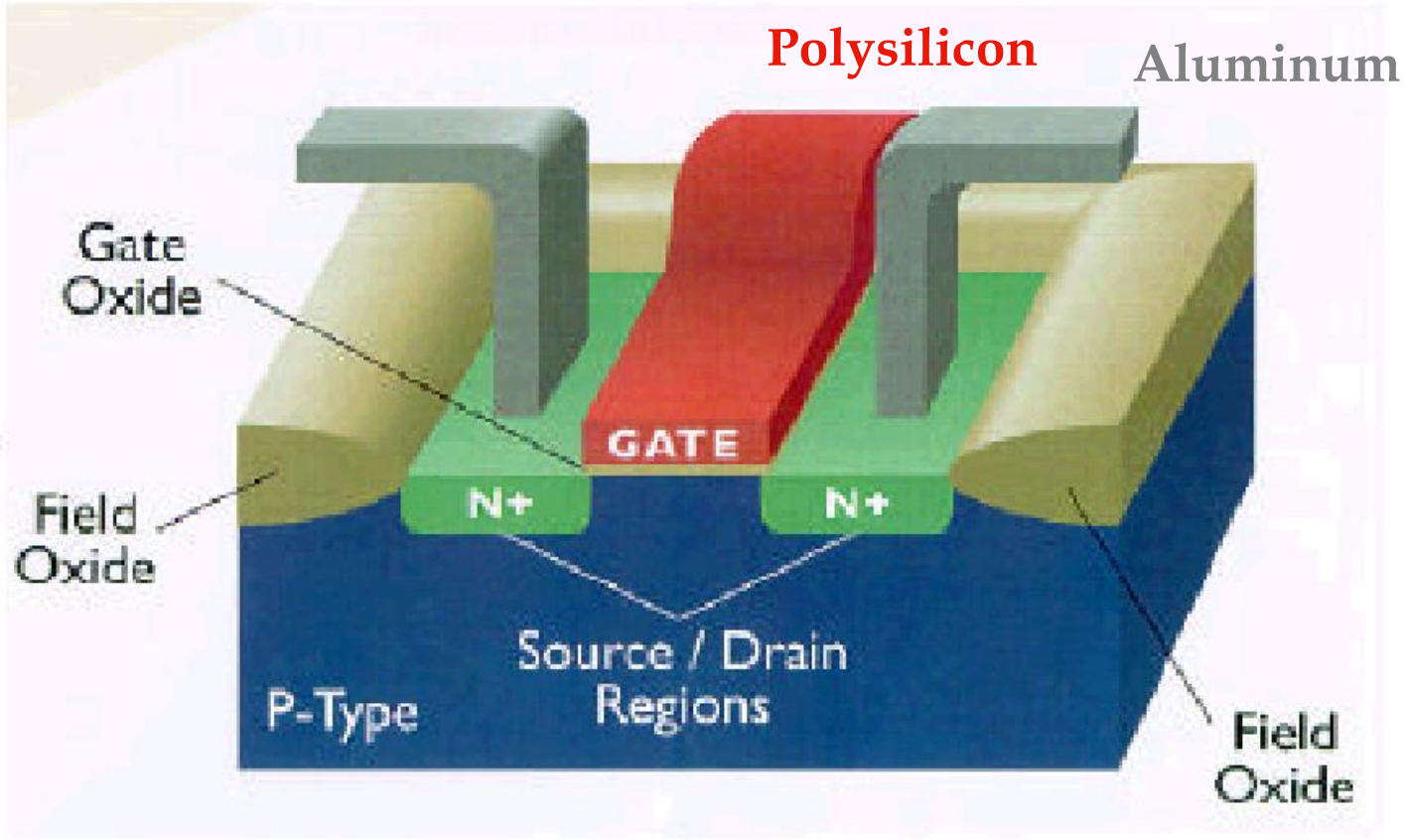
INTRODUCTION TO FULL-CUSTOM LAYOUT (Chapter 2)

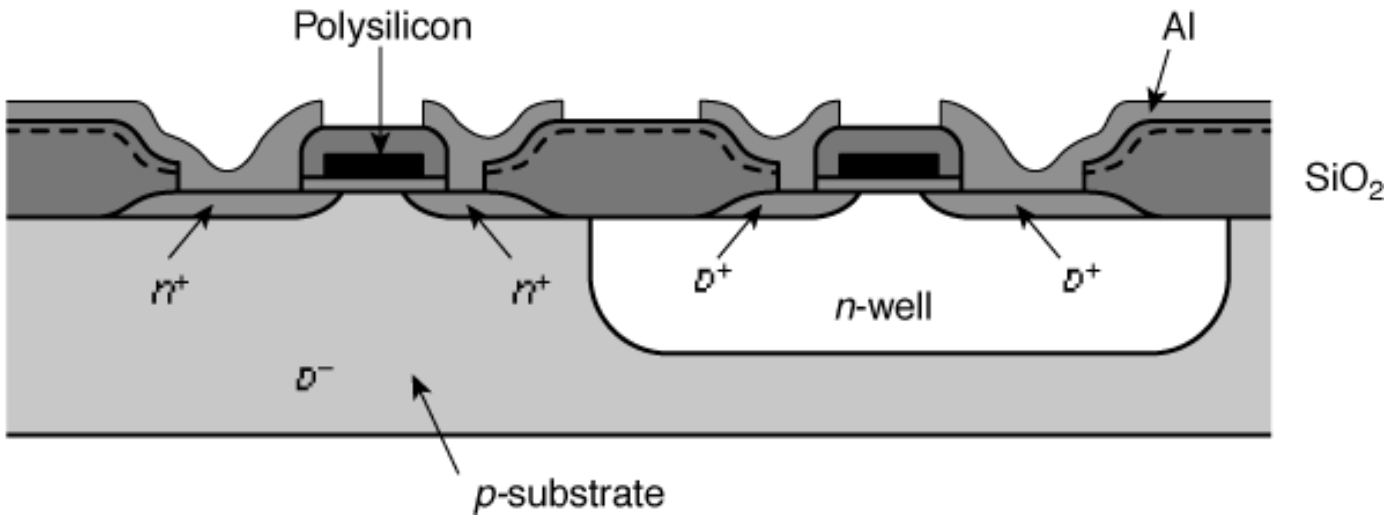
AND THE *MAGIC* LAYOUT TOOL

3D Perspective



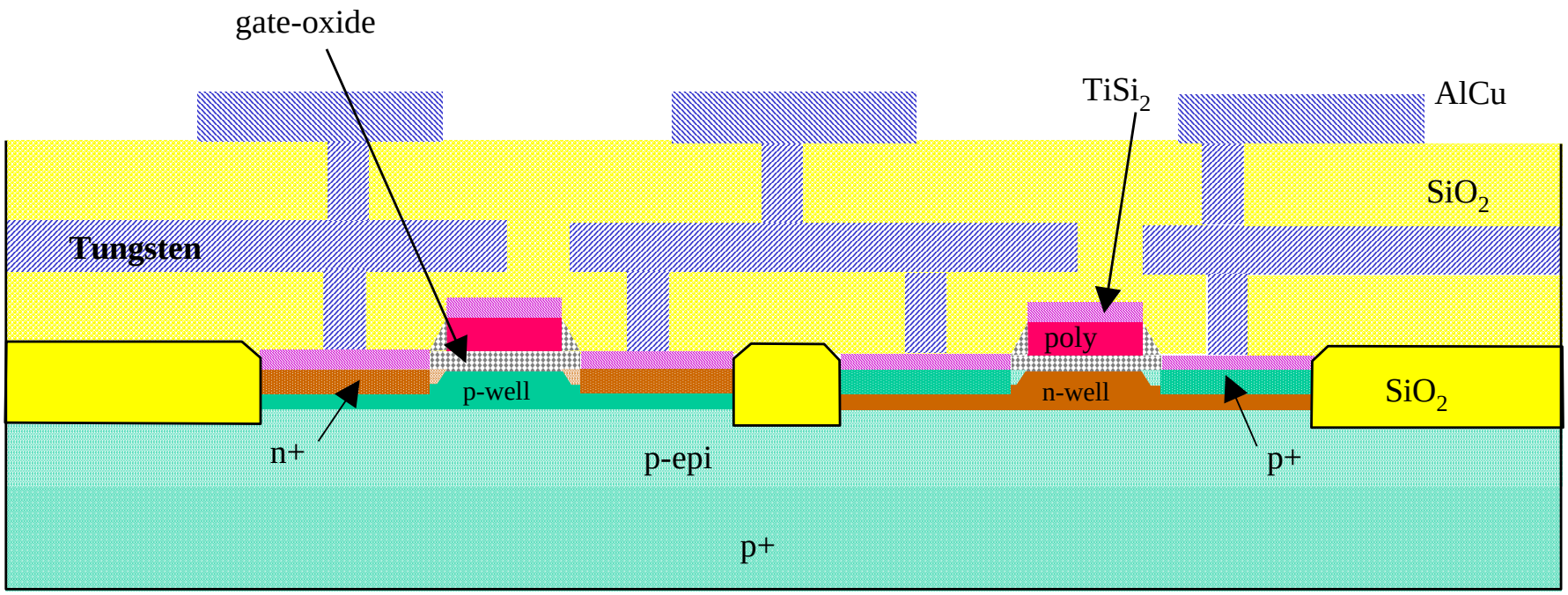
Source: Digital Integrated Circuits, 2nd ©

CMOS Process



Source: Digital Integrated Circuits, 2nd ©

A Modern CMOS Process

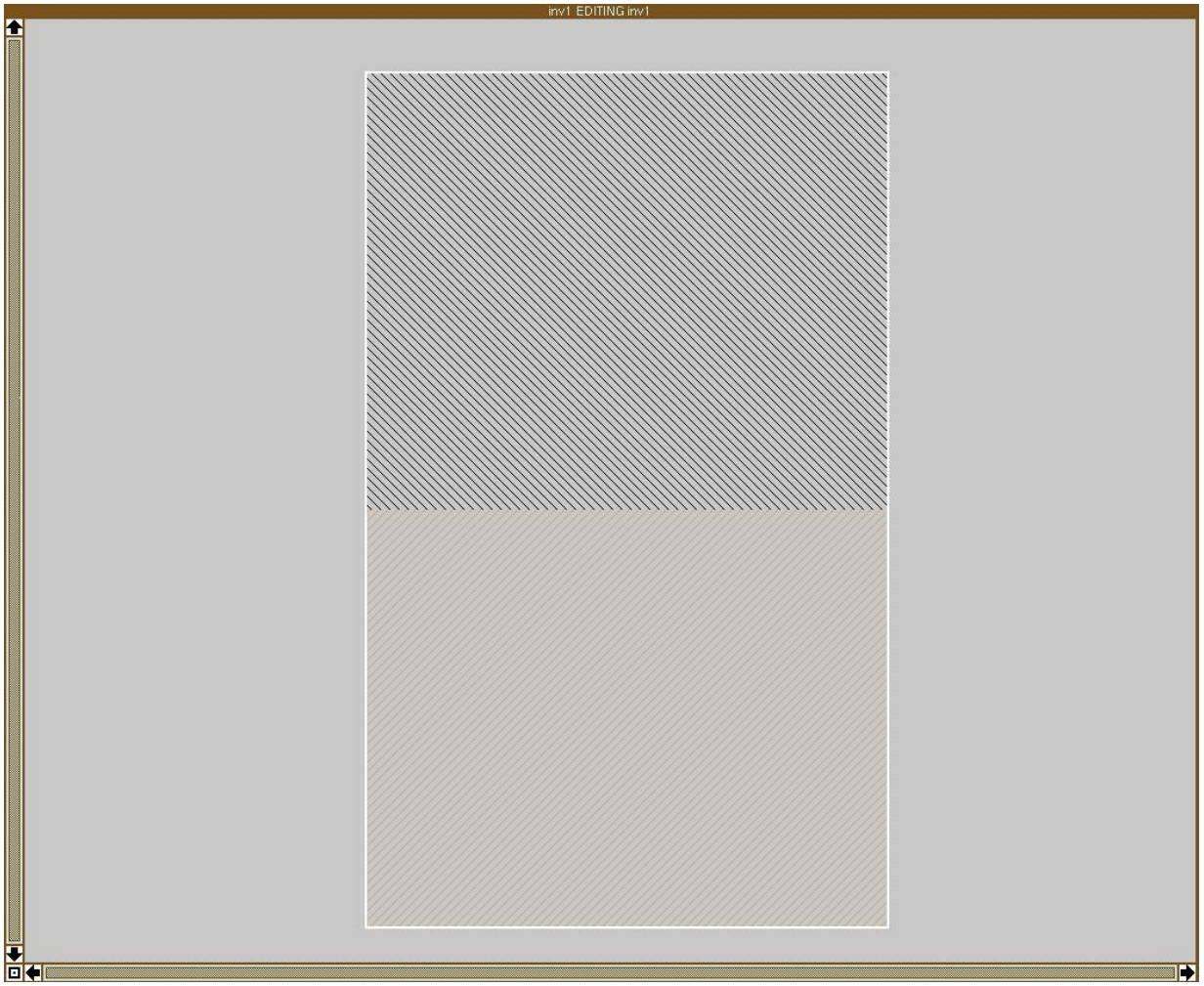


Dual-Well Trench-Isolated CMOS Process

Source: Digital Integrated Circuits, 2nd ©

nwell and pwell

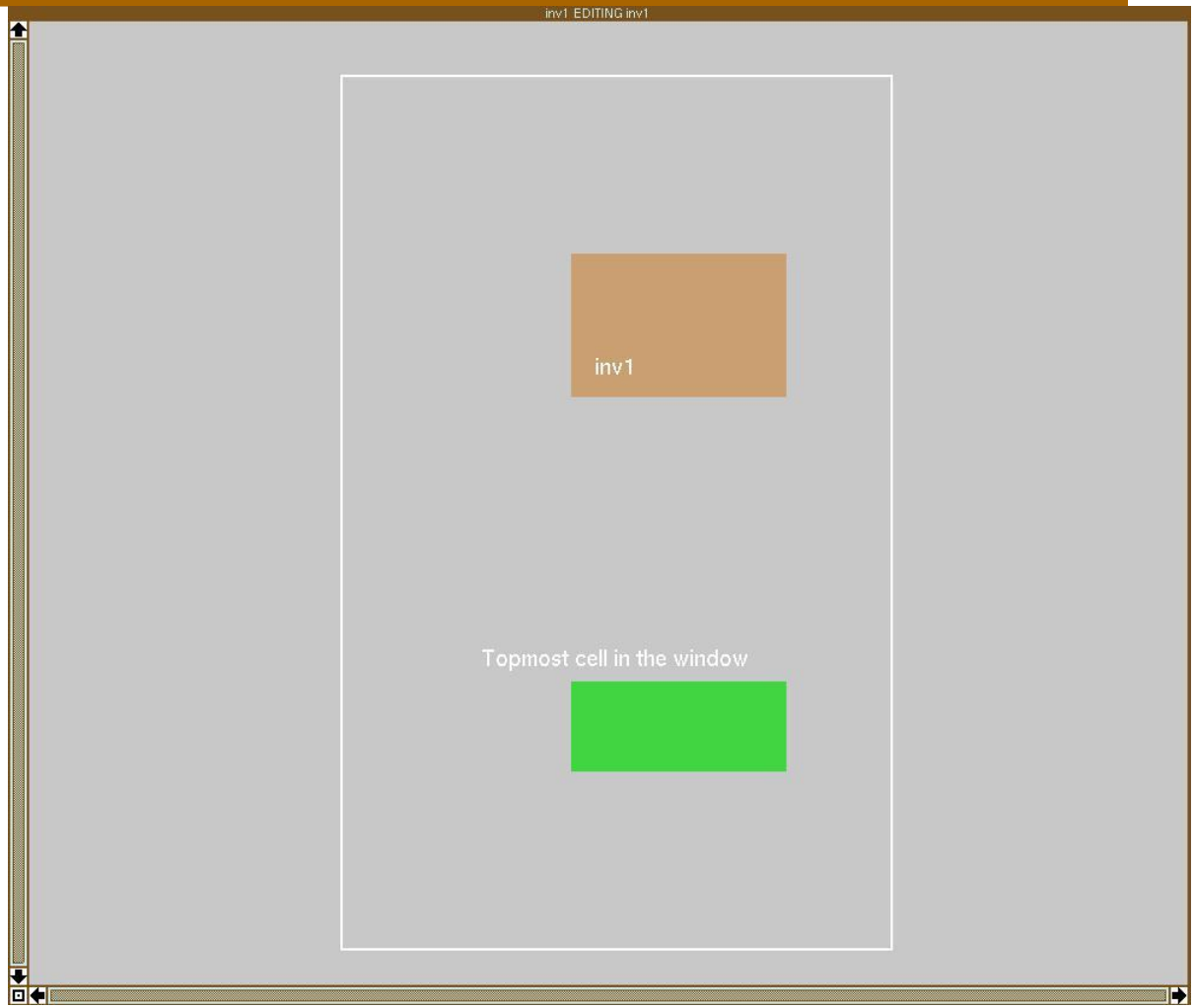
- The "bodies" of the transistors



Source: Omar Sattari

ndiffusion and pdiffusion

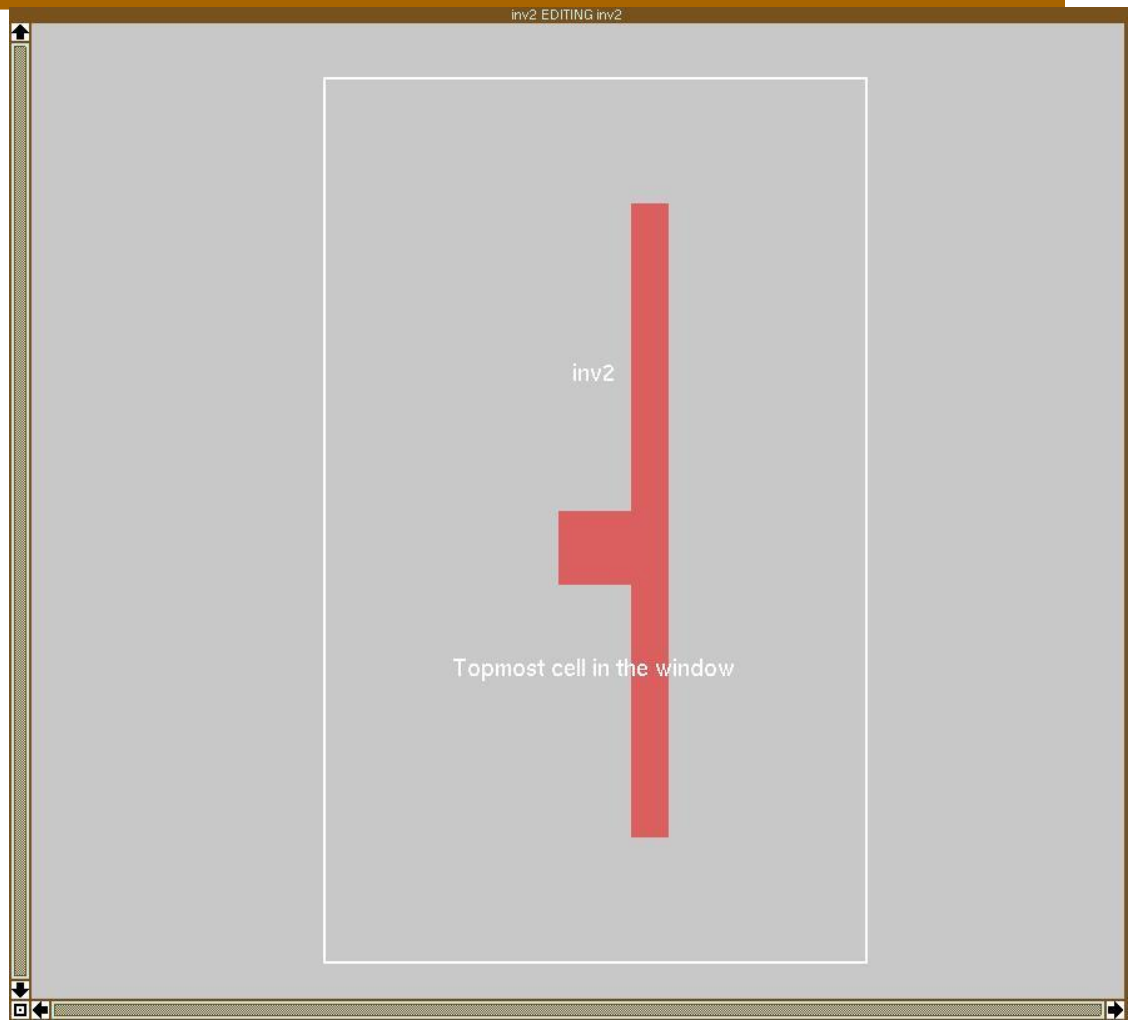
- Source and Drain for each transistor



Source: Omar Sattari

Polysilicon

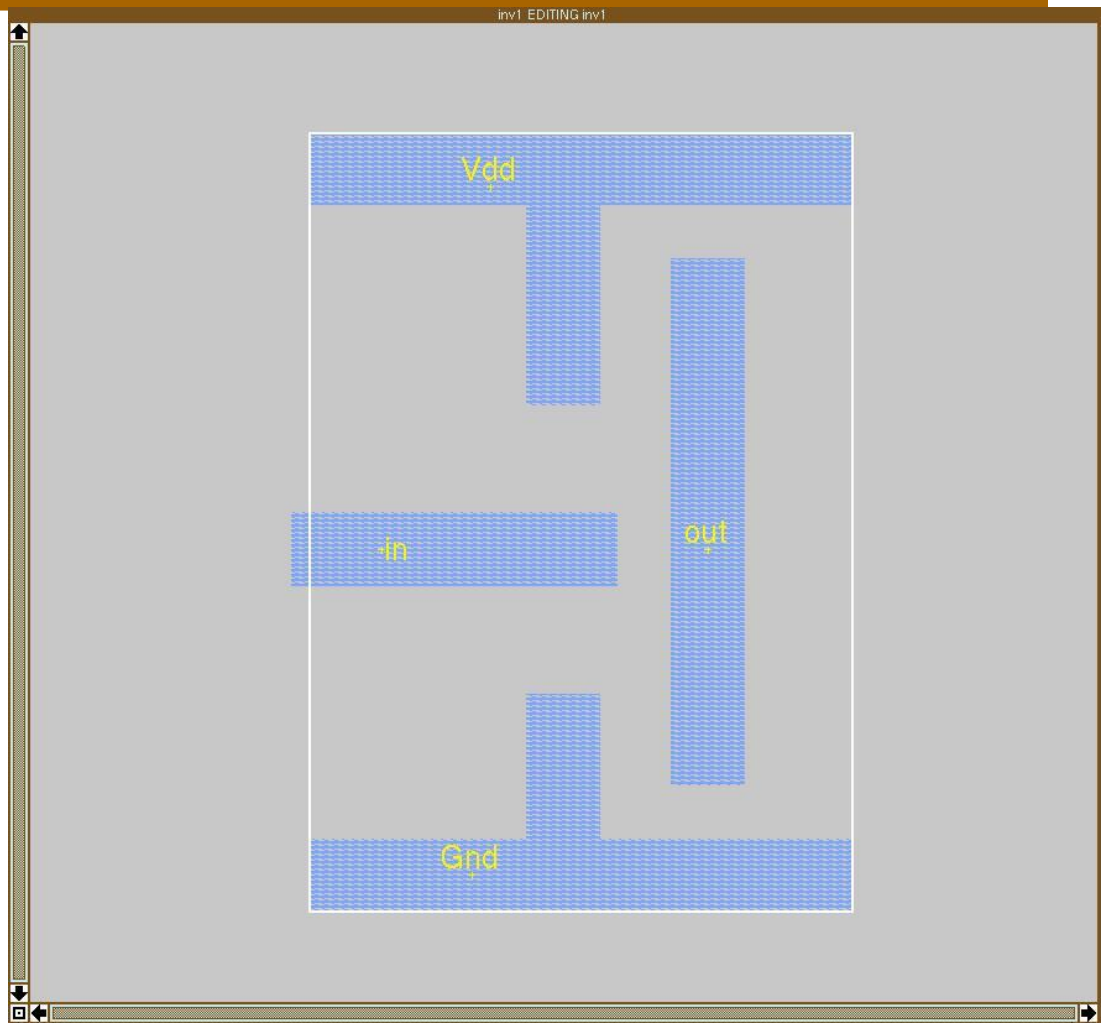
- Gate of transistors and for short-distance wiring



Source: Omar Sattari

metal1

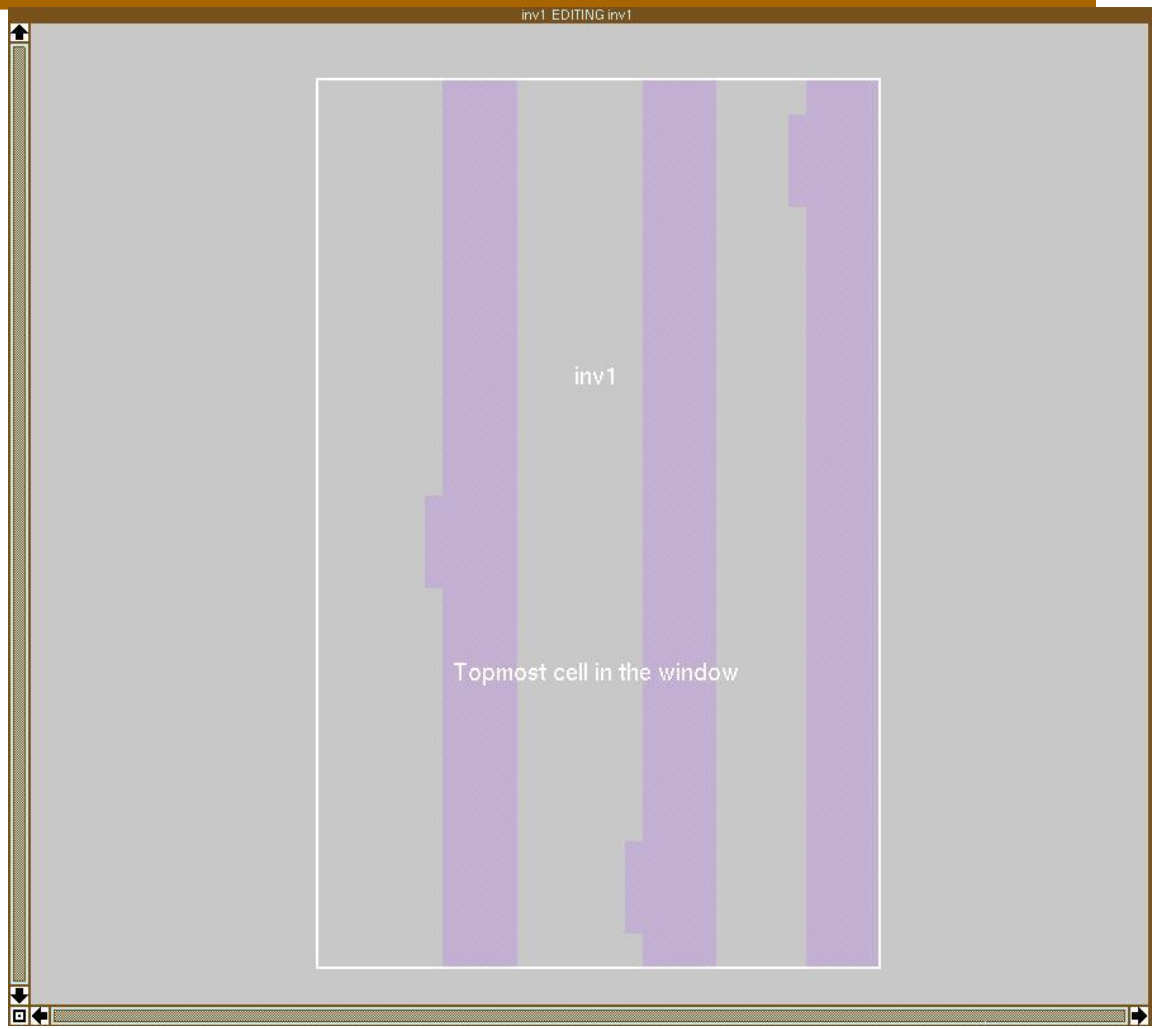
- First level of interconnect



Source: Omar Sattari

metal2

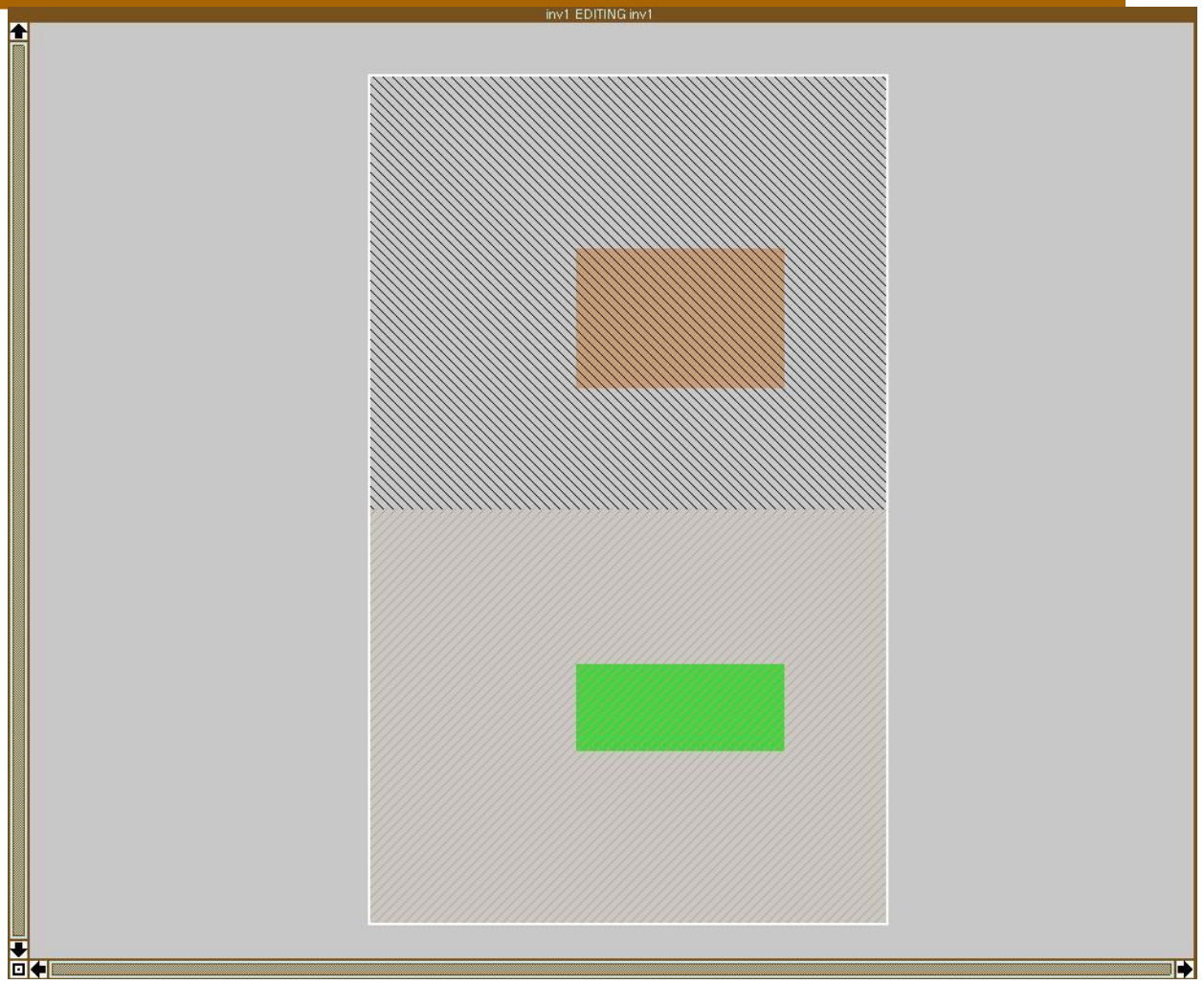
- Second layer of interconnect



Source: Omar Sattari

Building an Inverter: Starting with Well and Diffusion

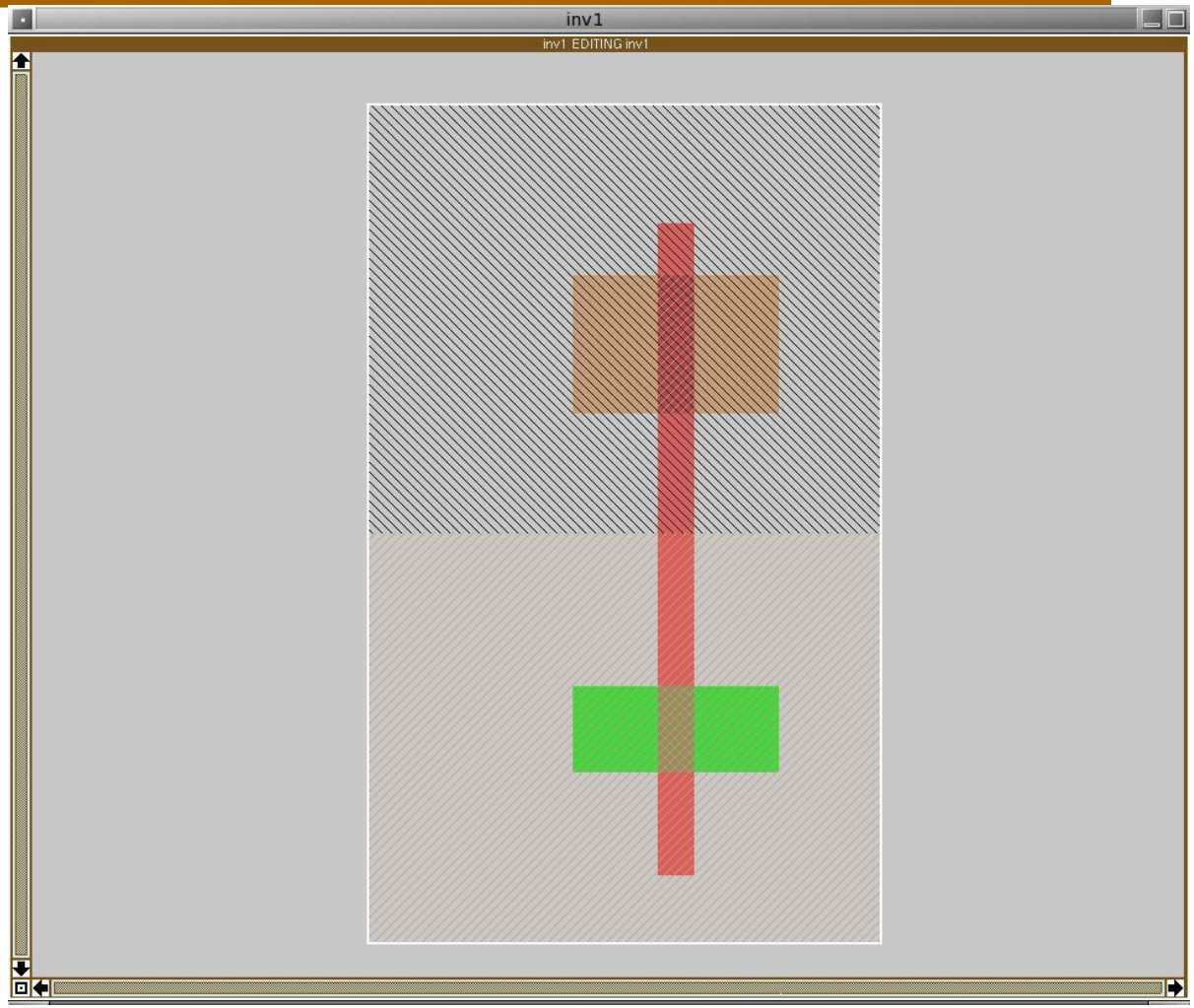
- Place N-type and P-type diffusions
  - Convention is to place PMOS on top and NMOS on bottom



Source: Omar Sattari

Transistors

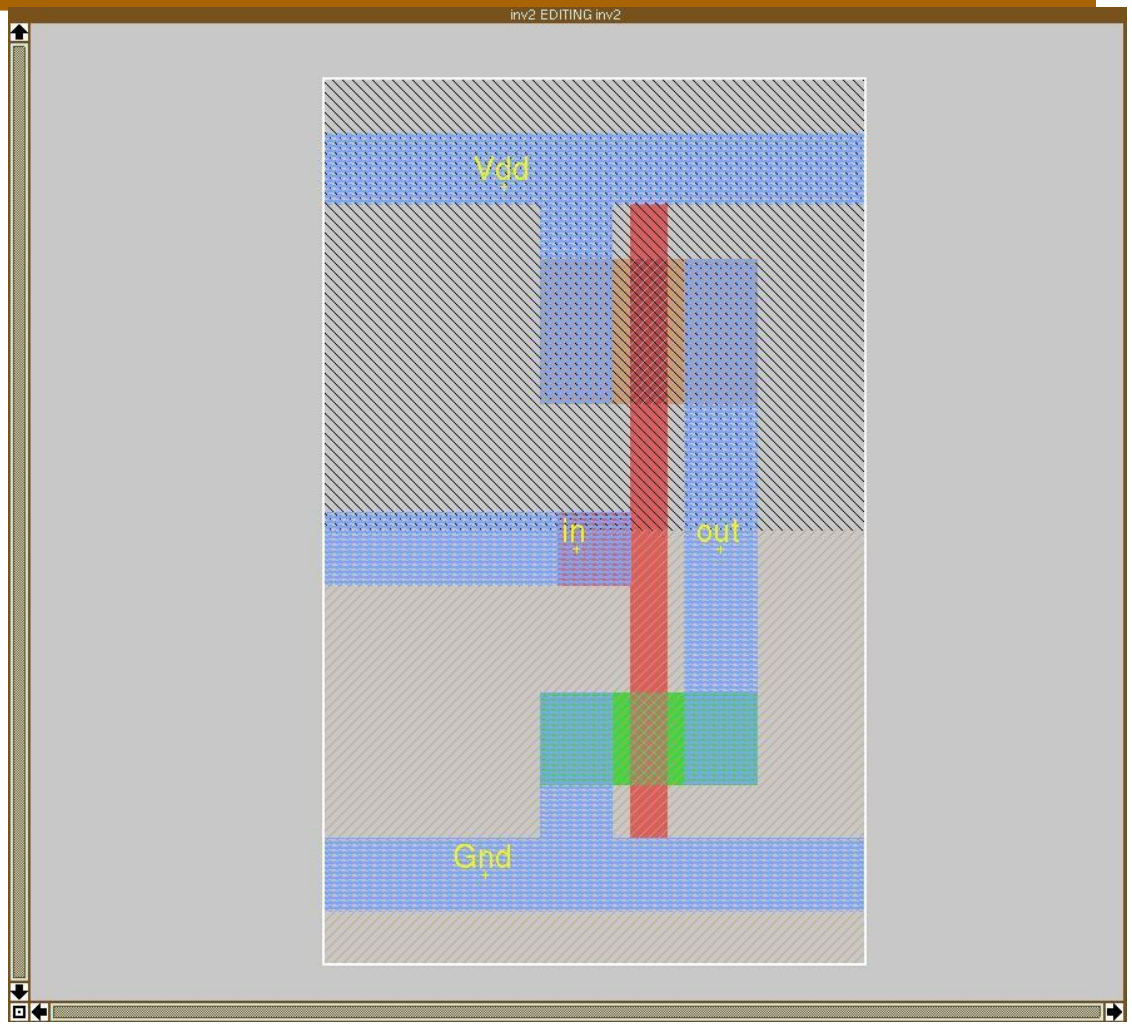
- poly crossing diffusion produces a transistor!
- Common gate here
- PMOS shown on top
- NMOS shown on bottom



Source: Omar Sattari

metal1

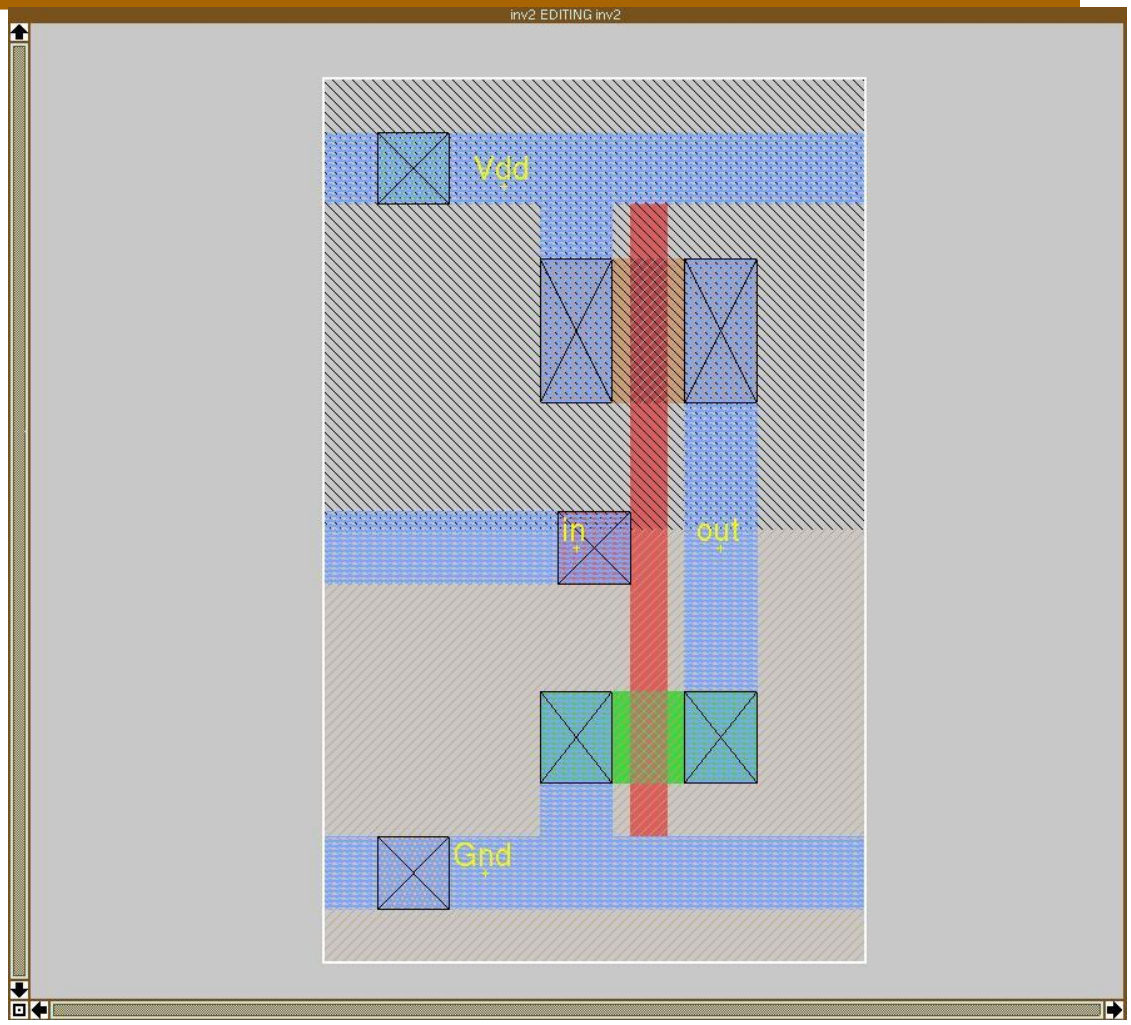
- metal1 laid down but not yet connected
- Use metal for *Vdd* and *Gnd*
- Labels added
  - Extremely useful for testing
  - Documents design
  - Use "point" labels, not large area ones
  - Never use *global* labels that end in an "!"



Source: Omar Sattari

metal1 contacts

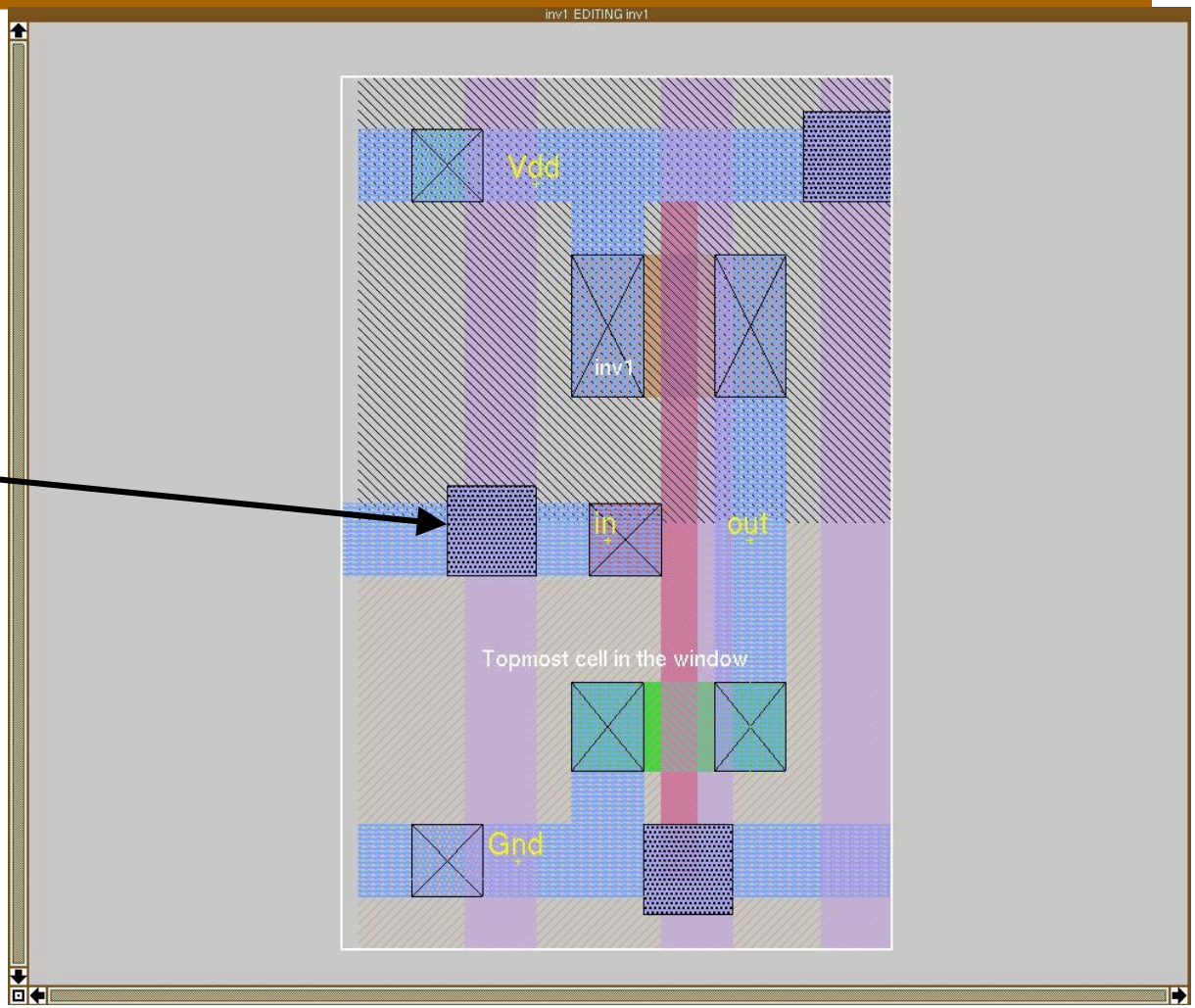
- Connections now made between metal1 and:
  - pdiff
  - ndiff
  - poly
  - nwell
  - pwell
- Each via/contact is a different layer in magic



Source: Omar Sattari

metal2

- Use metal2 for longer distance routing
- Routes over the "top" of other circuits shown
- metal2 contacts connect metal1 and metal2 only



Source: Omar Sattari