Layout Guidelines

1. Orientation of Vdd/Gnd lines in schematics

2. Orientation of transistors
   * Transistors "vertical"
     + Narrow pitch
   * Transistors "horizontal"
     - Limited room to stack transistors
     + Easier to make wide transistors

3. Stacking transistors

   Example:
   - Narrow pitch

   Much better to "shrink definition"!
   - Smaller area

B. Baas
4) Routing of Vdd/Gnd
   - (in metal) Poly probably never, drill only for short distances

* - metal 1
  + Very convenient
  + Most common

- metal 2
  + Signals can easily go under power/ground

- Use wider wires (6x7 for buse) + large (many) contacts

5) (see p. 31)

6) Cell placement

- Vdd/Gnd wires line up

7) Metal routing discipline

Suppose we want to route across this cell vertically

Key point: every wire blocks perpendicular wires from using that layer

B. Baa
Rows of diffusion in a cell

**Two:**
- preferable

**Form:**
- often has large empty spaces
- easier for more complex cells
- harder to use with sub-height cells
- generally avoid it if possible
a) Guideline: Try to use only m1 and m2 in small cells

b) Guideline: Use only one direction for each layer.

Ex: (bad)

c) Guideline: Alternate directions for each layer

Ex: min. m1 = m3, m5

Ex: m2 = m4, m6

2) Stack vias: to reduce area

In old days, this was not possible

Ex: m1 to m3

Now thanks to C4P, vias can be stacked

Remember m2 is blocked!

Most processes can stack arbitrariness high but in magic:

pam12 c
m123 c
pam12c (padiff, m1, m2)

m234 c
mdiff12c (ndiff, m1, m2)

m345 c
m456 c
9. Reduce area

a) Share, overlap (Ex: Vdd and Gnd)

   Ex: parallel wires
   Vdd vs. Gnd
   Vdd 3 x
   Gnd 6 x

   Ex: 2 inverters

b) Abut

b) Better:

   FA FA FA FA
   vs.
   FA FA FA FA

   Better:

   (c) Avoid wires that turn corners, if possible

   i) ii) ii)

   "pitch matching"
   pitch of A cells matched with
   pitch of B cells
d) Consider shape of overall structure
   Ex: 32-bit adder

   * For an arbitrary block, a square shape will give the shortest total wire length

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e) Transistor folding (for large devices)

   Ex:  

   - Large source & drain caps.
   - With very wide trans., will not fit inside the allotted cell height

   * Fold transistor

   - Source cap is larger (good)
   - Drain cap is reduced (good)
Reduce max. delay

\[ t_p = 0.69 \times \frac{R_{\text{mos}}}{C_L} \]

- Reduce \( R_{\text{mos}} \)
  - In layout, means wider transistors
  - This increases load cap. for driving gate
  - Helps a lot for under-driven nets, diminishing returns eventually

- Reduce \( C_L \)

  - Shorter wires \( \rightarrow \) Smaller area \( \rightarrow \) Lower \( C_L \) \( \rightarrow \) Reduce fanout

  \( \rightarrow \) Smaller area ...

  * Use higher-level metals if possible
Reduce power

\[ P = CV^2 f \]

* Reduce \( C \)

\( V \) and \( f \) generally set by other requirements

Other more complex techniques possible