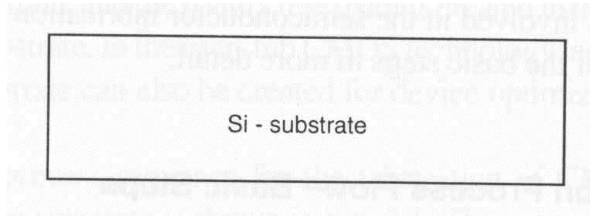
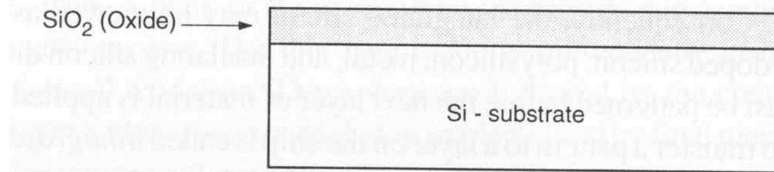
THREE FABRICATION EXAMPLES

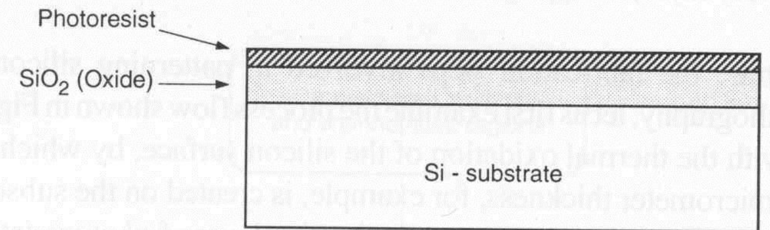
Fabrication Example 1

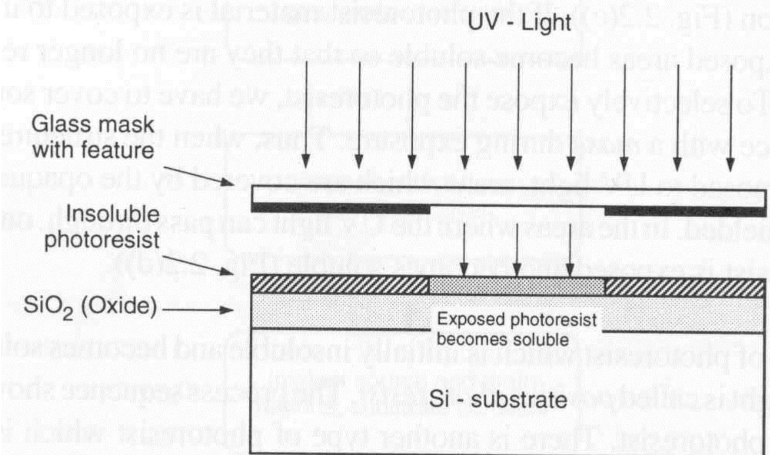
- The example shows a 2-D side view of the fabrication steps for the following
  - A single NMOS transistor
  - Metal1 contacts
  - Metal1 layer

Fabrication – Patterning of SiO_2





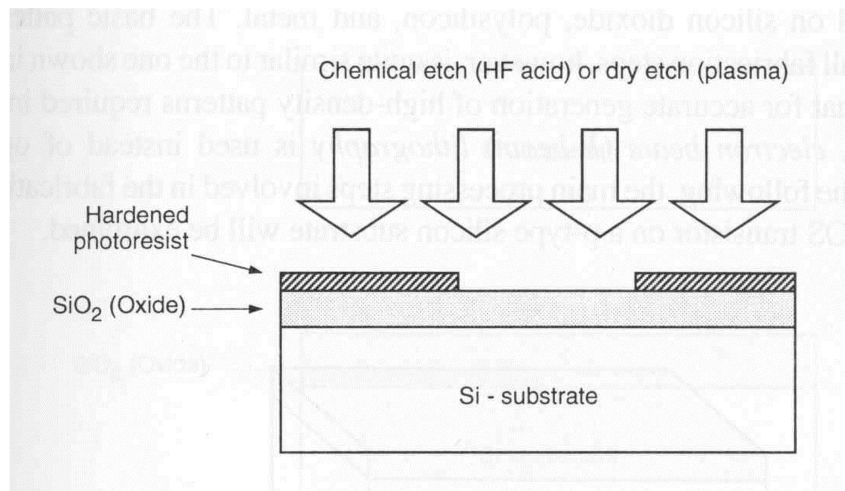


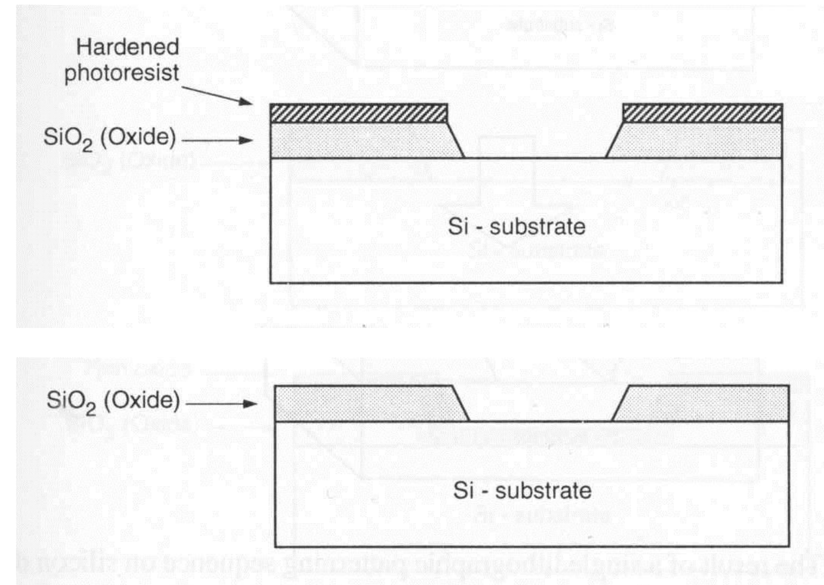


- Grow SiO_2 on Si by exposing to O_2
  - high temperature accelerates this process
- Cover surface with photoresist (PR)
  - Sensitive to UV light (wavelength determines feature size)
  - Positive PR becomes soluble after exposure
  - Negative PR becomes insoluble after exposure

Source: CMOS Digital Integrated Circuits

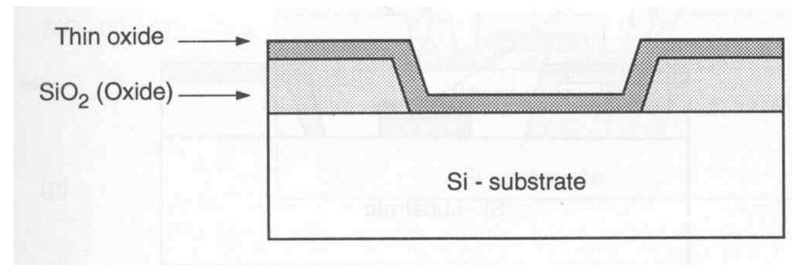
Fabrication – Patterning of SiO_2





- Photoresist removed with a solvent
- SiO_2 removed by etching (HF)
- Remaining photoresist removed with another solvent

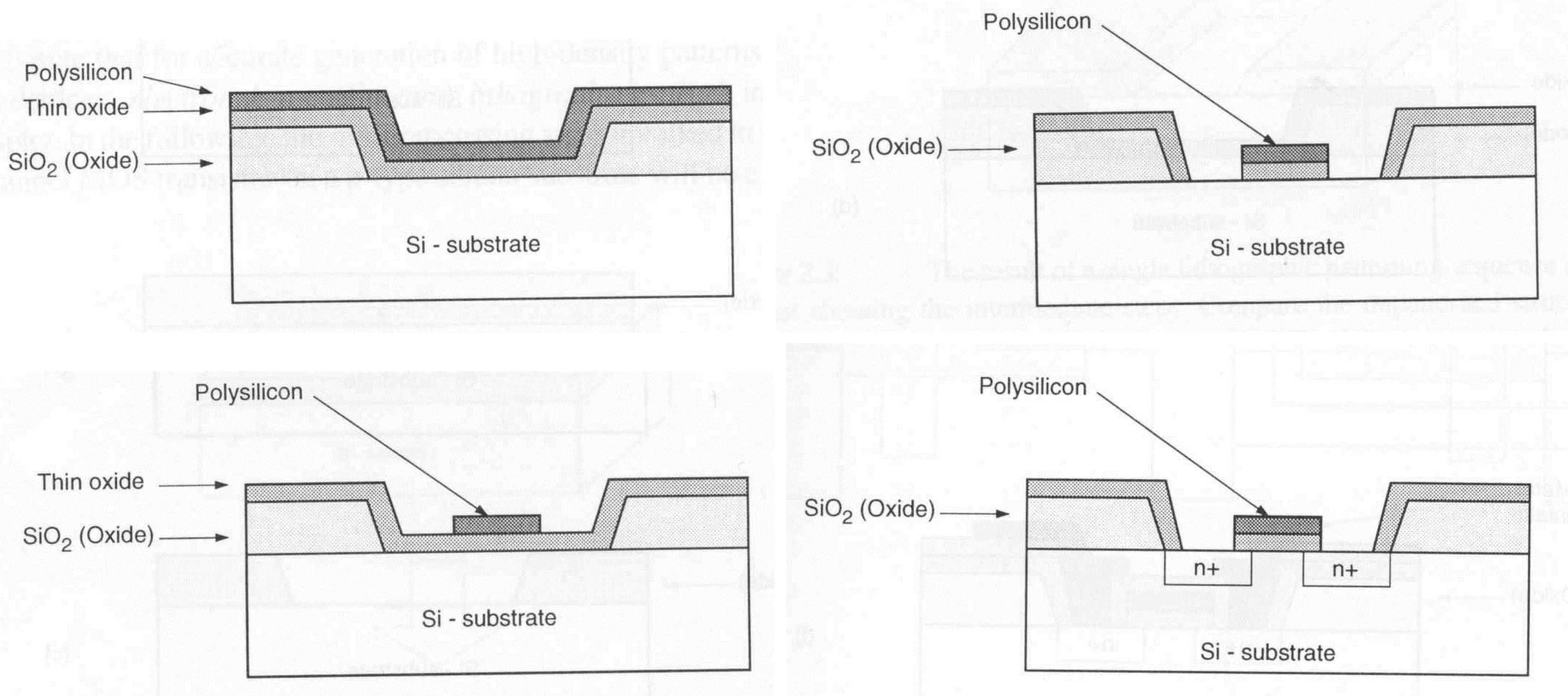
NMOS Transistor Fabrication



- Thick field oxide grown
- Field oxide etched to create area for transistor
- Gate oxide (high quality) grown

Source: CMOS Digital Integrated Circuits

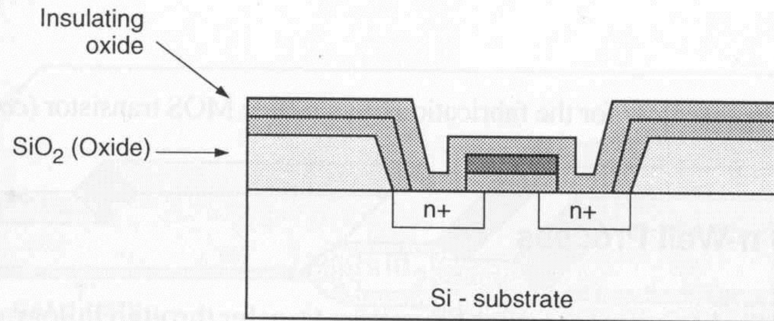
NMOS Transistor Fabrication

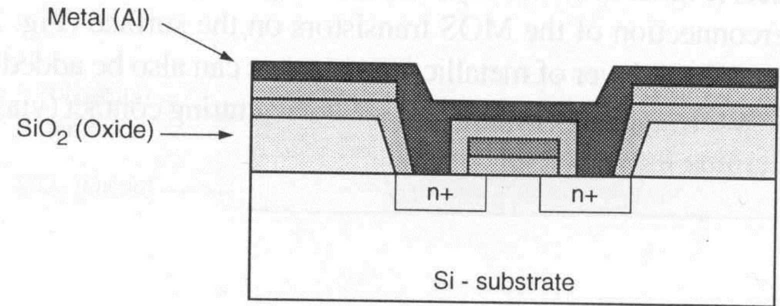


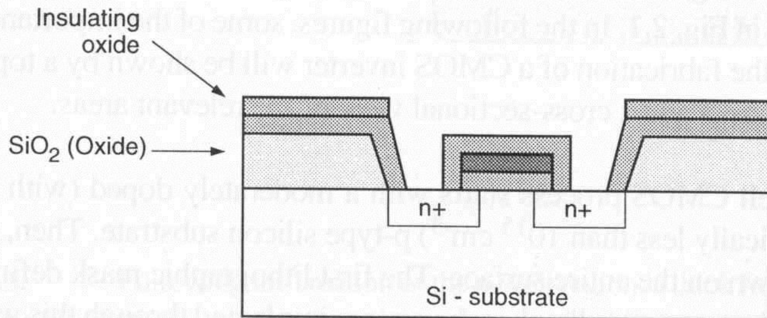
- Polysilicon deposited (doped to reduce R)
- Polysilicon etched to form gate
- Gate oxide etched from source and drain
  - Self-aligned process because source/drain aligned by gate
- Si doped with donors to create n+ regions

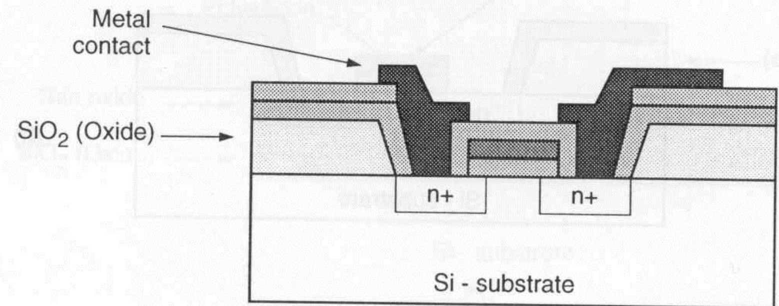
Source: CMOS Digital Integrated Circuits

NMOS Transistor Fabrication









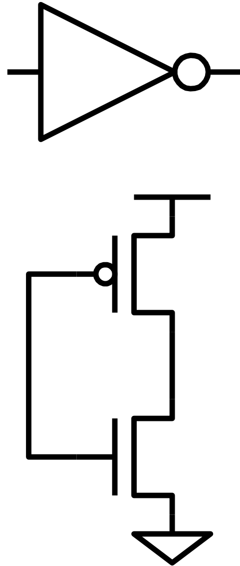
- Insulating SiO_2 grown to cover surface/gate
- Source/Drain regions opened
- Aluminum evaporated to cover surface
- Aluminum etched to form metal1 interconnects

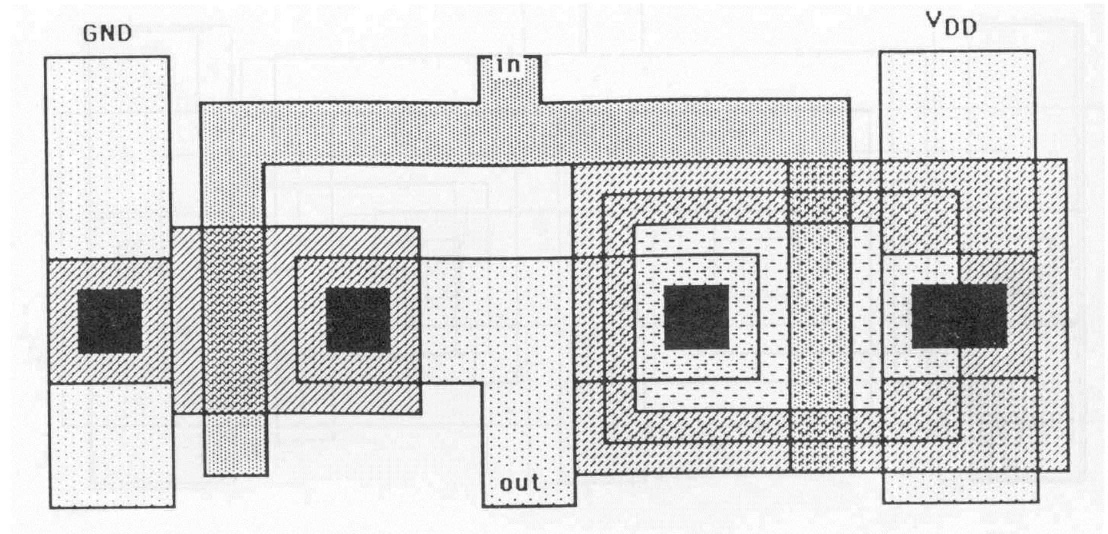
Source: CMOS Digital Integrated Circuits

Fabrication Example 2

- The example shows a 3-D view of the fabrication steps for the following
  - A CMOS inverter
    - A single NMOS transistor
    - A single PMOS transistor
  - Metal1 contacts
  - Metal1 layer

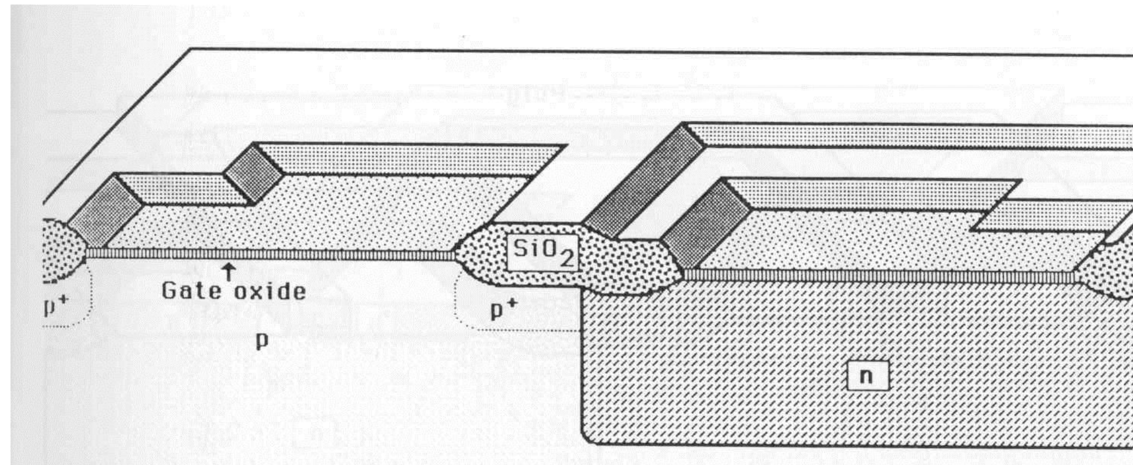
Inverter Fabrication





- Inverter
  - Logic symbol
  - CMOS inverter circuit
  - CMOS inverter layout (top view of lithographic masks)

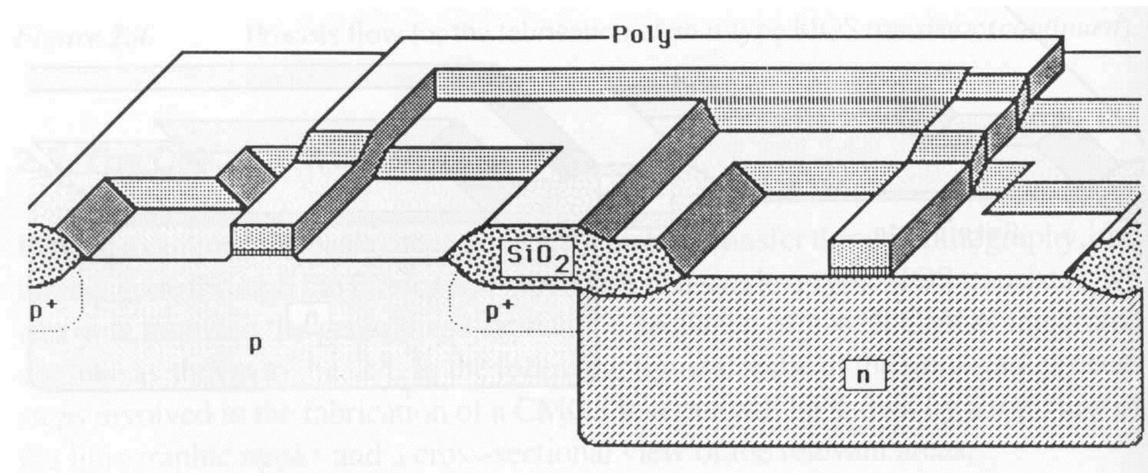
Inverter Fabrication



- N-wells created
- Thick field oxide grown surrounding active regions
- Thin gate oxide grown over active regions

Source: CMOS Digital Integrated Circuits

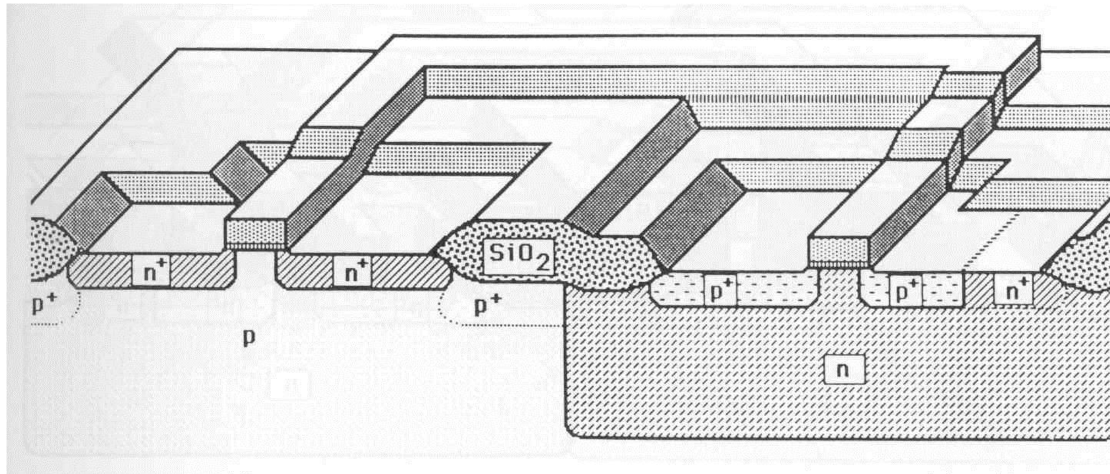
Inverter Fabrication



- Polysilicon deposited
  - Chemical vapor deposition(Places the Poly)
  - Dry plasma etch(Removes unwanted Poly)

Source: CMOS Digital Integrated Circuits

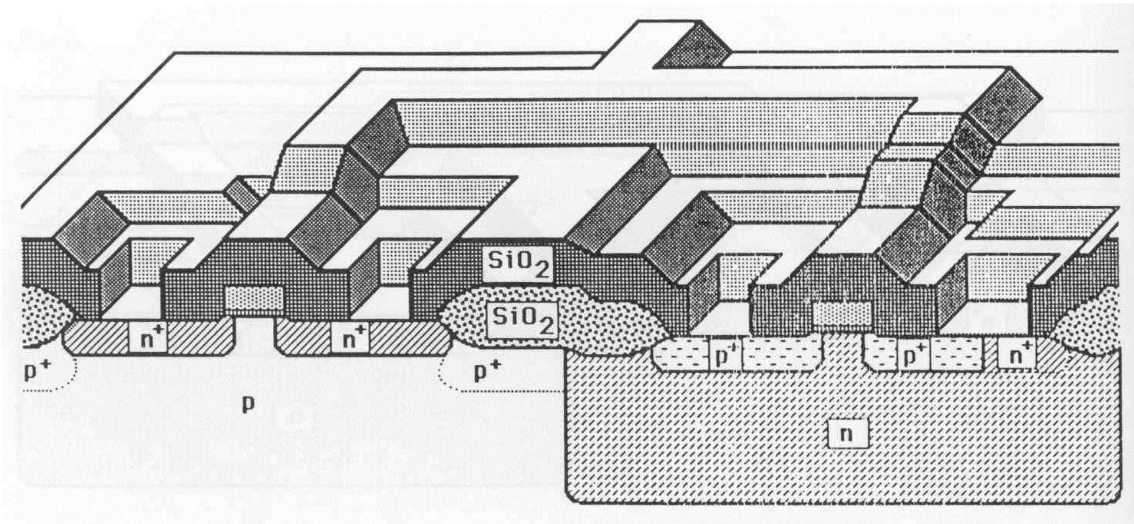
Inverter Fabrication



- N+ and P+ regions created using two masks
  - Source/Drain regions
  - Substrate contacts

Source: CMOS Digital Integrated Circuits

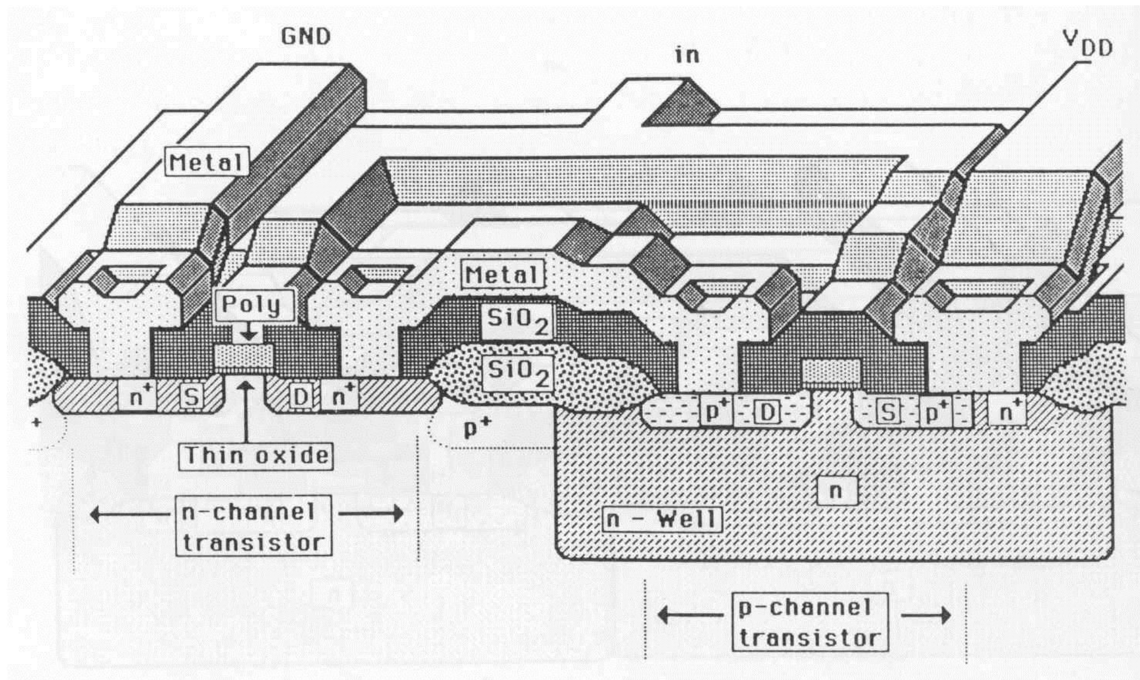
Inverter Fabrication



- Insulating SiO_2 deposited using CVD
- Source/Drain/Substrate contacts exposed

Source: CMOS Digital Integrated Circuits

Inverter Fabrication



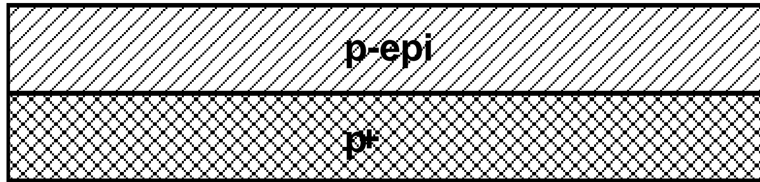
- Metal (Al) deposited using evaporation
  - Meta1 contacts made with Aluminum here
- Metal patterned by etching

Source: CMOS Digital Integrated Circuits

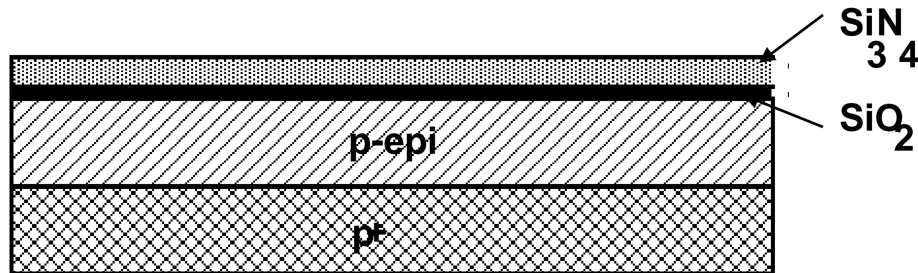
Fabrication Example 3

- The example shows a 2-D side view of the fabrication steps for the following
  - A CMOS inverter
    - A single NMOS transistor
    - A single PMOS transistor
  - Metal1 contacts
  - Metal1 layer
  - Metal2 vias
  - Metal2

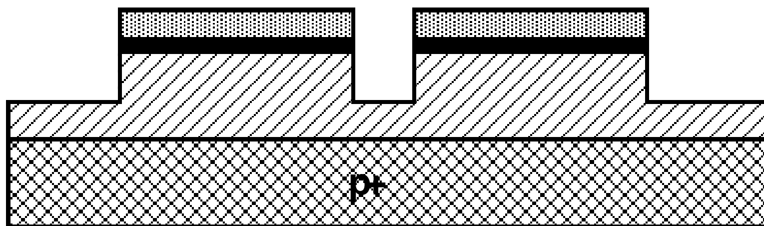
CMOS Process Walk-Through



(a) Base material: p+ substrate with p-epi layer



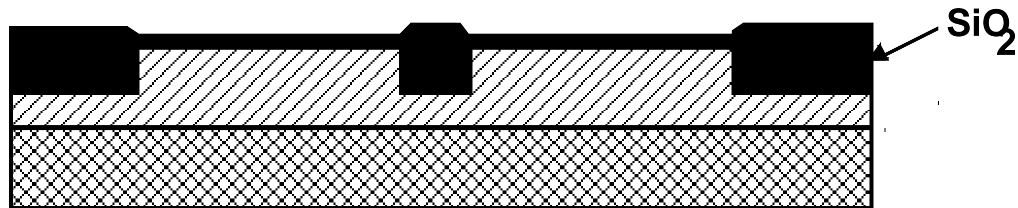
(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)



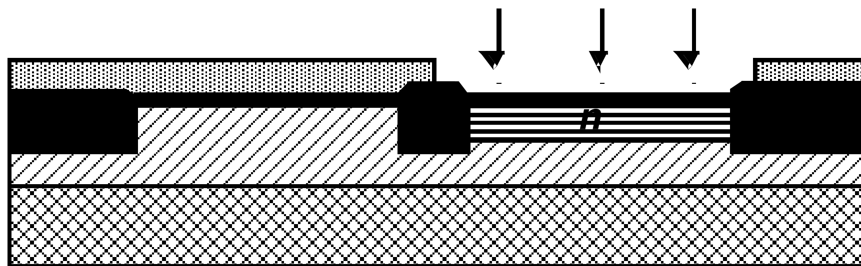
(c) After plasma etch of insulating trenches using the inverse of the active area mask

Source: Digital Integrated Circuits, 2nd ©

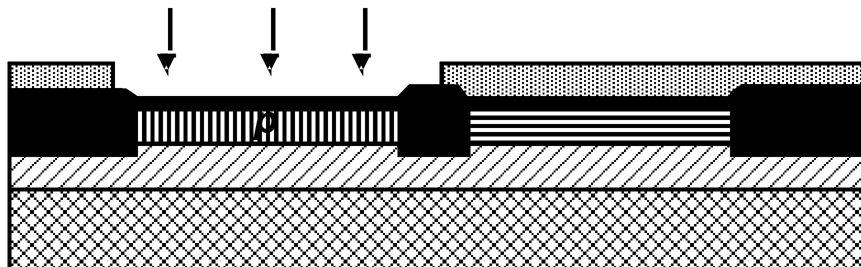
CMOS Process Walk-Through



(d) After trench filling, CMP planarization, and removal of sacrificial nitride



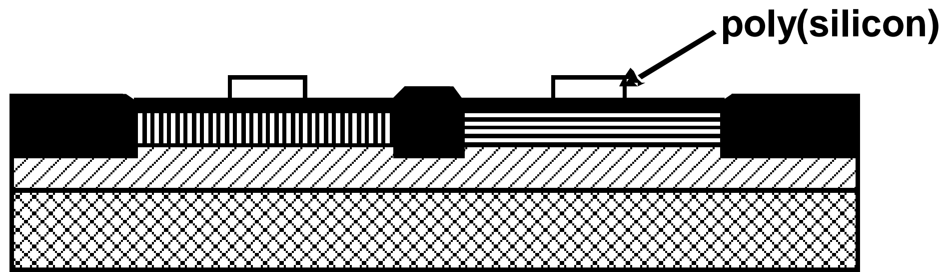
(e) After n-well and V_{Tp} adjust implants



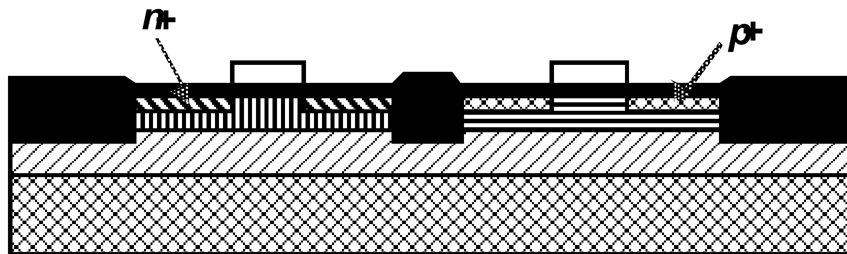
(f) After p-well and V_{Tn} adjust implants

Source: Digital Integrated Circuits, 2nd ©

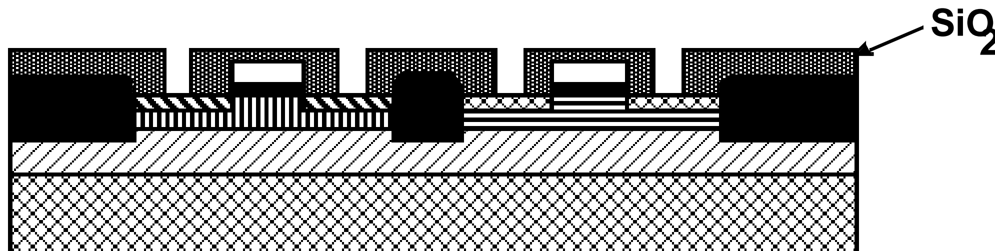
CMOS Process Walk-Through



(g) After polysilicon deposition and etch



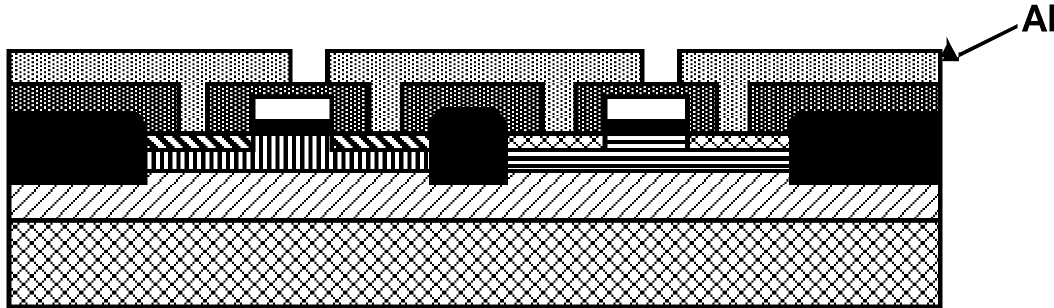
(h) After *n*+ source/drain and *p*+ source/drain implants. These steps also dope the polysilicon.



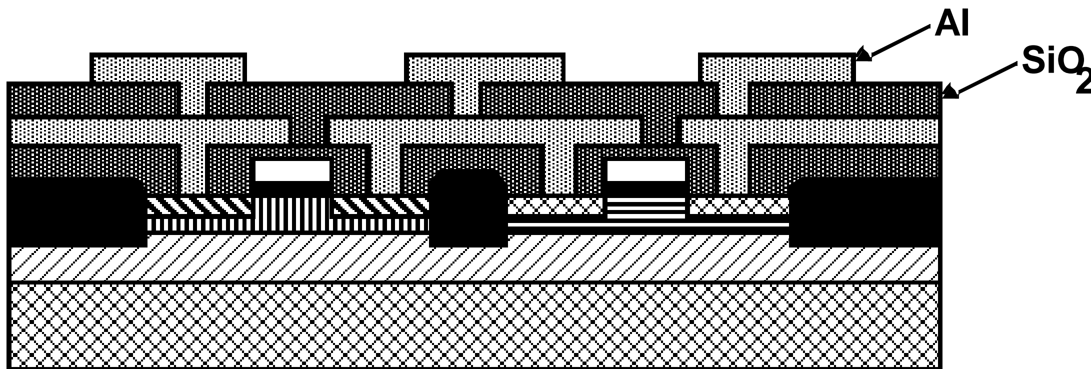
(i) After deposition of SiO_2 insulator and contact hole etch.

Source: Digital Integrated Circuits, 2nd ©

CMOS Process Walk-Through



(j) After deposition and patterning of first Al layer.



(k) After deposition of SiO_2 insulator, etching of via's, deposition and patterning of second layer of Al.

Source: Digital Integrated Circuits, 2nd ©