INTRODUCTION TO VLSI FABRICATION MATERIALS & PROCESSES
7 Primary Chip Ingredients

1) Silicon – crystalline
   - Near-perfect crystal (atoms organized in a regular, ordered lattice)
   - Semiconductor—not a conductor or insulator, but somewhere in between and its conduction can be altered significantly

2) SiO\textsubscript{2} – Silicon dioxide
   - Just like it says, made from silicon and oxygen
   - Insulator

3) Silicon – polycrystalline, poly, polysilicon
   - Silicon but only small regions are organized as crystalline structures. Polysilicon structures are made up of multiple small crystalline regions where the smaller regions are not aligned with each other.

4) n-type dopants
   - Materials that contain 5 outer electrons
   - “donors”
   - Examples: phosphorus, arsenic
7 Primary Chip Ingredients

5) p-type dopants
   - Materials that contain 3 outer electrons
   - "acceptors"
   - Examples: boron, gallium

6) Metal wires
   - In older technologies, made of aluminum. Now copper is commonly used because of its lower resistivity.
   - Conductors

7) Contacts/vias
   - Tungsten and aluminium commonly used
   - These are "vertical" connections between layers
The 3D Nature of Chips

6) Metal wire layers

7) “vertical” contacts/vias

• By convention we typically describe chips as being in the orientation with the substrate “horizontal” and interconnect layers placed on top of the substrate.
5 Primary Fabrication-Materials and Fabrication-Processes

1) Photoresist
   - *Positive photoresist* (becomes soluble when exposed to UV light)
   - *Negative photoresist* (becomes insoluble when exposed to UV light)
   - Applied roughly 1 μm thick to entire wafer

2) Etching processes
   - The “selectivity” of different etches varies in the sense that the materials that are etched or not etched depends on the particular etch.
   - Acid (wet etching). Ex: HF acid
   - Plasma (dry etching)
Etching of Polysilicon

Source: Device Electronics for Int. Circuits
3) Masks – one per patterned shape
   • Picture a developed film negative used to make photograph prints; or a slide

5 Primary Fabrication-Materials and Fabrication-Processes

3) Masks – one per patterned shape
   - The mask may contain one or more copies of the same chip (20 in this example)
   - The chip layer’s image is typically several times larger in the mask compared to the final chip size

https://en.wikipedia.org/wiki/Photomask
4) Laying down material
   A. Deposition
      • Example method: CVD
      • Example materials: SiO$_2$, silicon
   B. Growth
      • Example materials: SiO$_2$ on silicon substrate
   C. Implantation
      • Produces high dopant concentration regions
      • Diffusion implantation
         – Silicon exposed to dopant gas at high temperature
      • Ion implantation
         – Dopant ions are implanted at high speed with an accelerator
         – Causes lattice damage
         – Normally followed by annealing step (short high temperature “crystal healing” process)
      • Example implanted structures: source/drains, transistor channels, well and substrate contacts, polysilicon
   D. Sputtering – for metals
5) Planarization – extreme flattening of the wafer’s surface
• Suppose we have the case below where similar patterns stacked on top of each other produce large vertical features.

Cracks more easily and has high resistance on vertical portions.
5) Planarization – extreme flattening of the wafer’s surface

- CMP: Chemical Mechanical Planarization (or Polishing)
- Needed for reliability and consistent thickness of a large number of interconnect layers
Basic repeated process

1) Deposit a material
2) Coat with photoresist
3) Expose photoresist to a pattern of UV light using a light source and a patterned *mask*
4) Remove soluble photoresist with selective etching
5) Remove material below photoresist with selective etching (base material only)
6) Remove remaining photoresist with selective etching (hardened photoresist only)
Typical operations in a single photolithographic cycle (from [Fullman]).