DESIGN RULES

Design Rules

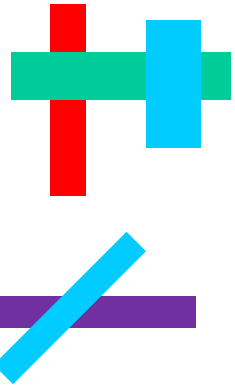
- There are two main interfaces between the chip designer and the process (CMOS fabrication) engineer
  1) **Design Rules** – Rules for constructing fabrication masks
  2) Chip design file
     a) GDSII – binary format, universally used today
     b) CIF – text readable format, used primarily by academic tools in the past
- Units commonly used in design rules
  1) absolute dimensions (micron rules)
  2) scalable design rules: lambda (λ) parameter (used in magic)
- Common rule examples:
  - minimum width of an object
  - minimum separation between two objects made of the same material
  - minimum separation between two objects made of different materials

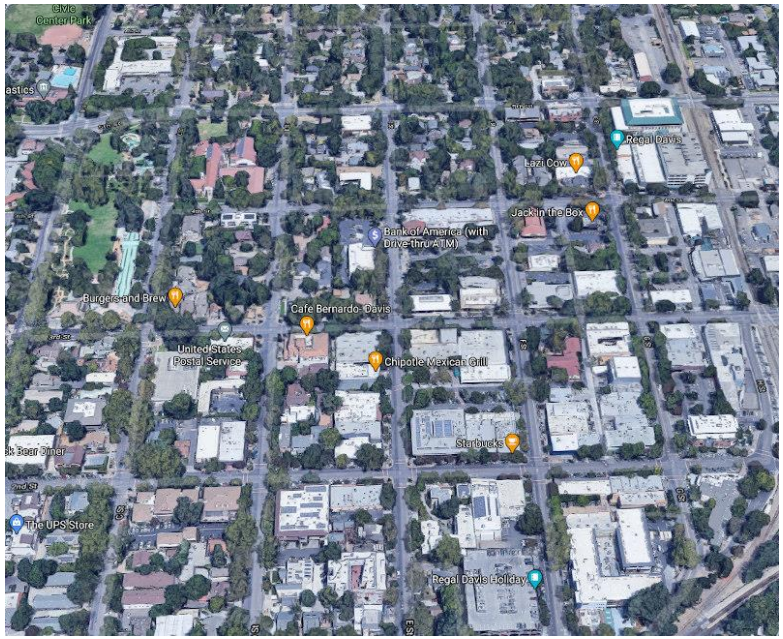
Scalable Design Rules

- "Lambda-based" scalable design rules
  - Allows full-custom designs to be easily reused by simple scaling from technology generation to technology generation
  - Lambda is roughly one half the minimum feature size
    - "1.0 μm technology" -> 1.0 μm min. length, lambda = 0.5 μm
    - "0.5 μm technology" -> 0.5 μm min. length, lambda = 0.25 μm
  - For our class, we are using a 0.18 μm technology so lambda is 0.09 μm
  - Mead and Conway, *Introduction to VLSI Systems*, 1978
- See course website for a link to our scalable design rules on the MOSIS website
- We are using "SCMOS_DEEP" rules written by MOSIS

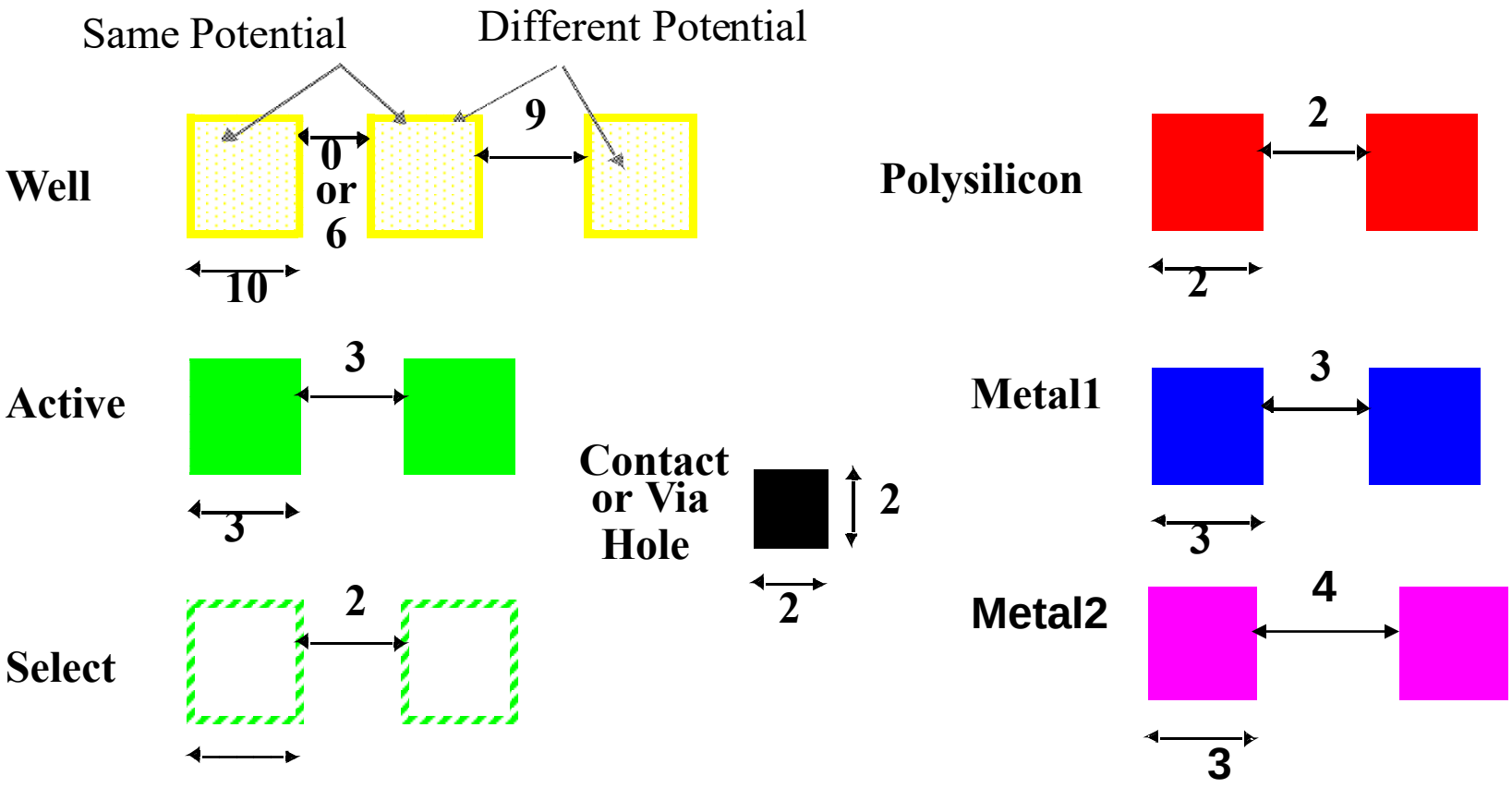
Manhattan Layout

- All features on modern chips are rectangles (often called "polygons")
  - In the past, some researchers have allowed 45 degree features but this flexibility was always later abandoned
- To decrease the size of features and to greatly simplify design, modern chip designs limit rectangle orientations to two directions only: north-south, and east-west, or what is commonly called "Manhattan" layout





Example Intra-Layer Design Rules (widths, spacings)



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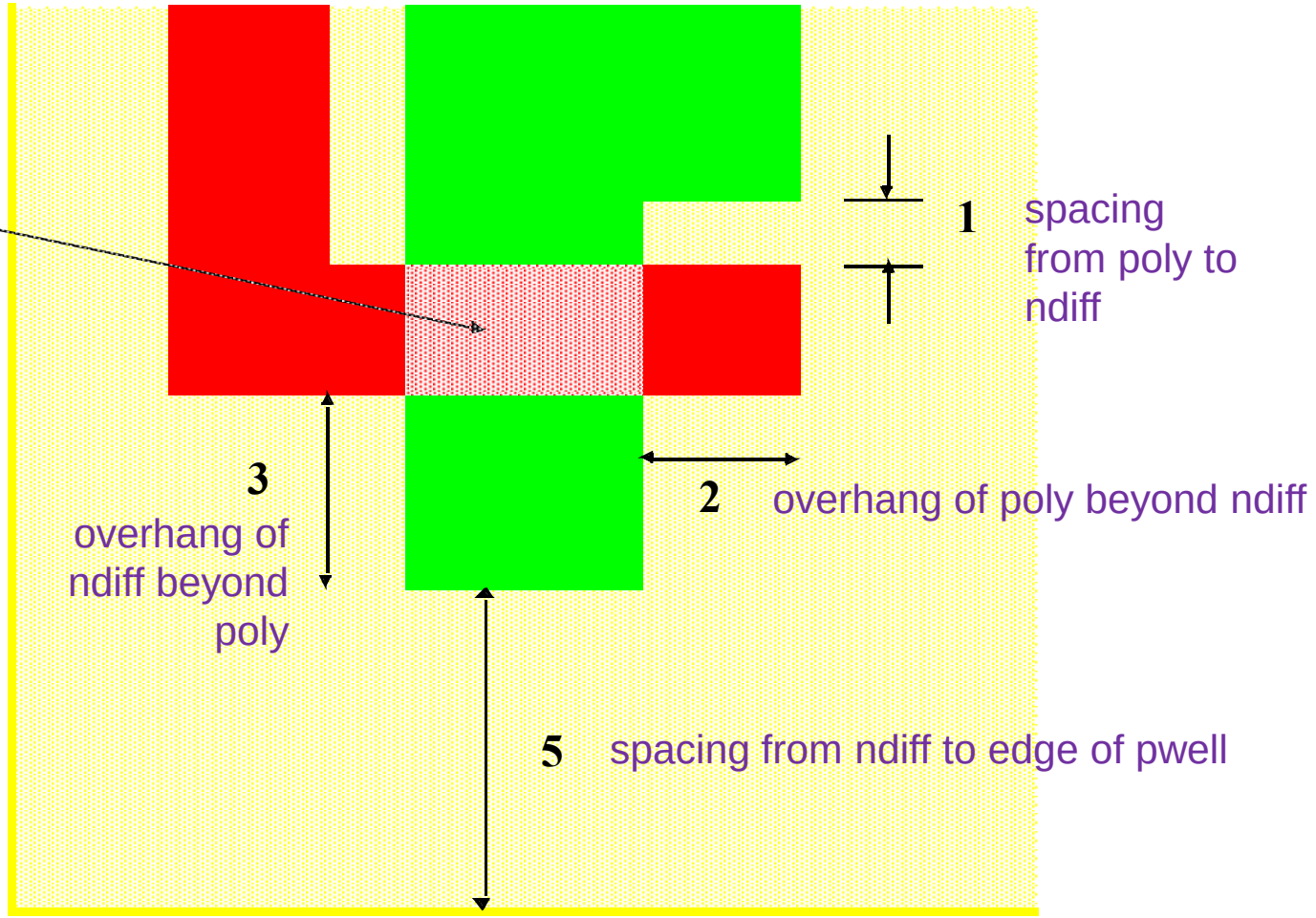
Example Design Rules: Transistor Layout

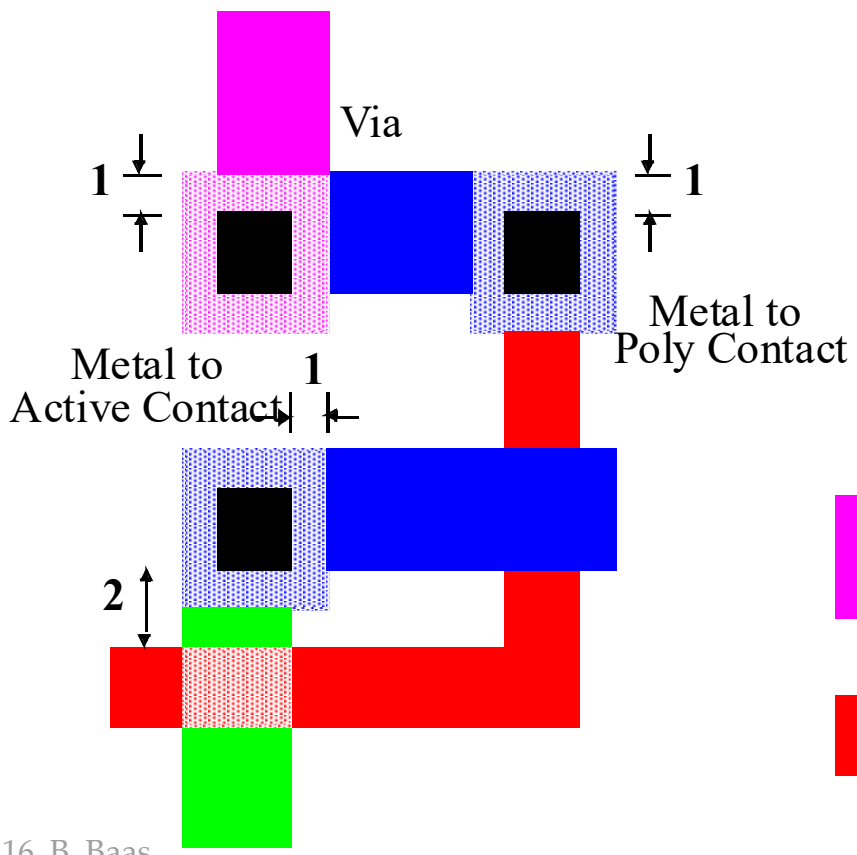


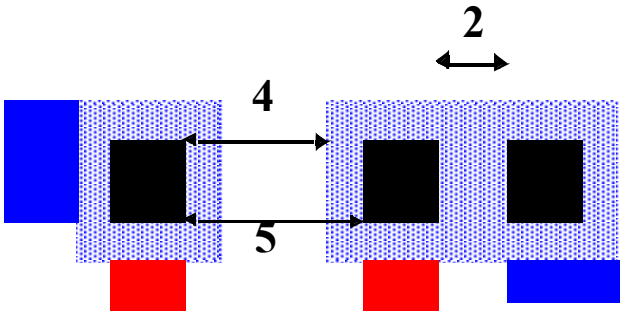
- red = polysilicon
- green = n-type diffusion
- yellow = pwell

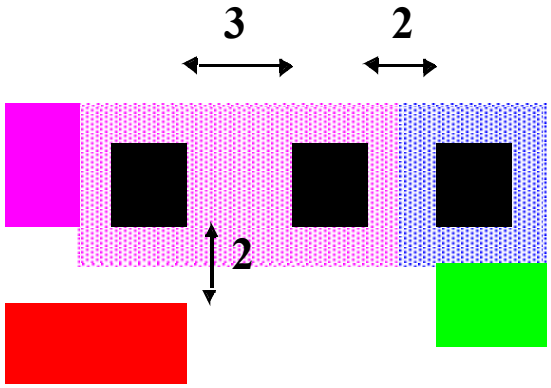
Source: Digital Integrated Circuits, 2nd ©

Example Design Rules: Vias and Contacts

- Note: contacts/vias appear differently than they do on magic

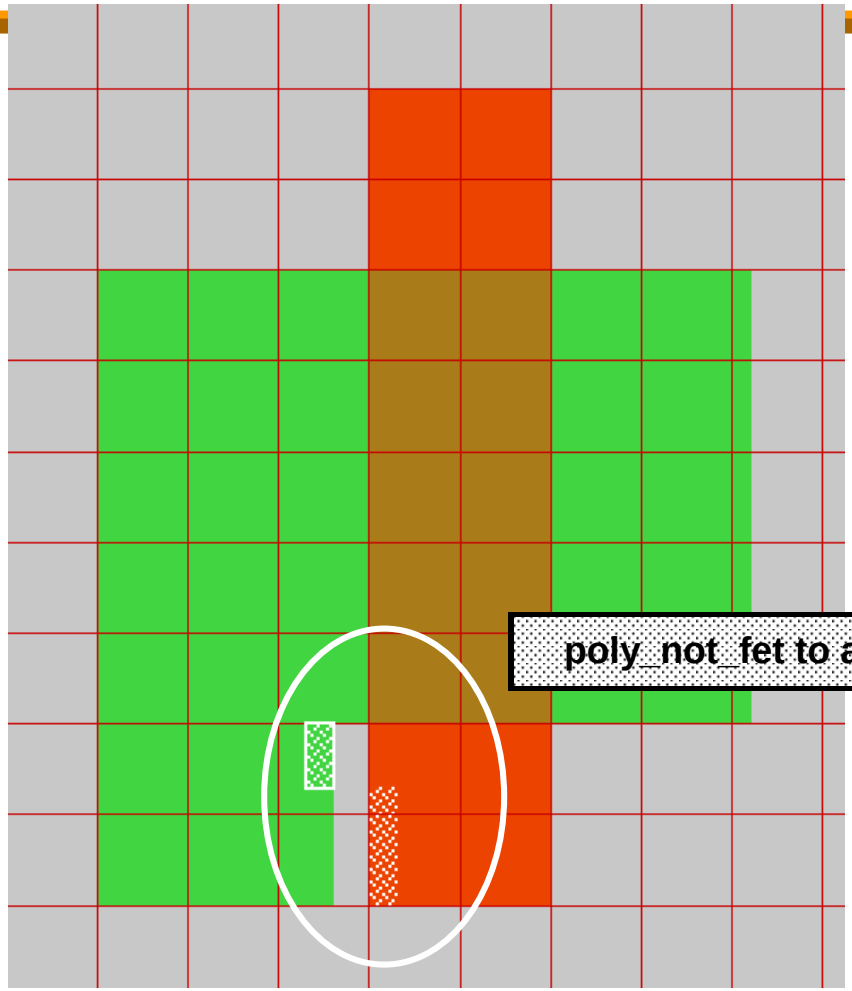






Source: Digital Integrated Circuits, 2nd ©

Design Rule Checker



In magic, white dots appear at the point of a DRC rule violation

Place a box around white dots and press “y” to see what is causing an error

Source: Digital Integrated Circuits, 2nd ©