Scaling Challenges of FinFET Architecture below 40nm Contacted Gate Pitch

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Introduction-The FinFET architecture, introduced at the 22nm node [1], has delivered improved MOSFET electrostatics, which has enabled gate-length (L_{Gate}) scaling down to 48nm Contacted Gate Pitch (CPP) at the 7nm node [2], [3] (Fig. 1). Enhanced performance gains have been realized via the 'Fin Effect' (W_{eff}/Fin-Pitch) boost, which provides improved drive current for a given capacitive load. However, limits on the Fin thickness are quickly being approached and will soon limit further L_{Gate} scaling, resulting in accelerated reduction in source/drain sizes vs. CPP. The combination of increasing Fin Effect and a plateau in the L_{Gate} place extreme pressure on the vertical conduction path from contacts to source and drain. With current values of contact resistivity (ρ_C) for metal-to-degenerately-doped silicon of ~2×10^{-9} [4] FinFET performance will significantly deteriorate below CPP of ~40nm, while a theoretical fully ohmic floor of ~$1\times10^{-10}\Omega$-cm^2 [5] could push the CPP limit to below 30nm. We conclude that there will be severe pressure for the industry to adopt a new device architecture or scaling option in the 30-40nm CPP region to carry on the power/performance benefits of CMOS scaling.

Discussion-Scaling trends for L_{Gate} and fin width vs CPP are shown in Fig. 2. Although, fin width plays a major role in L_{Gate} scaling, a faster scaling rate of L_{Gate} relative to fin width has been enhanced by fin profile improvements (Fig. 3). Given the near-ideal shape achieved at the 48nm CPP technology, further L_{Gate} reductions will not be achieved via this mechanism. The literature indicates a trend for increase subthreshold slope (SS) with scaling that is opposite that prescribed in the ITRS Roadmap (Fig. 4). This suggests that further L_{Gate} scaling may come at the expense of increased short-channel effects, which could halt future V_{dd} reductions. Increased DIBL below the CPP of 50nm (Fig. 4), indicates that FinFETs may be approaching the short-channel regime (SCR). This behavior can be explained by the ratio of gate to geometrical screening lengths (λ) as shown in Fig. 5. Effective current (I_{eff}) [6] is dominated by I_{ds} ($V_{gs}=V_{dd}$, $V_{ds}=V_{dd}/2$), and is limited by effective threshold voltage ($V_{th\text{-}eff}$) at $V_{ds}=V_{dd}/2$ for standard (RVT) CMOS. Fig.6 compares the $V_{th\text{-}eff}$ with ITRS roadmap requirements. A practical minimum power-supply-voltage ($V_{dd\text{-}min}$) can be estimated by ~$3\times V_{th\text{-}eff}$, which denotes that with all the effort to keep SS and DIBL small, $V_{dd\text{-}min}$ rises proportional to $log(1/L_{Gate})$, and L_{Gate} scaling opposes device performance. Therefore, electrostatics will be a major scaling challenge for FinFET technologies below CPP of ~50nm, tending to halt the L_{Gate} scaling.

Aggressive scaling of fin-pitch is driven by the need to reduce the parasitic capacitance components and to boost the performance elements such as 'Fin Effect' to effectively increase the drive current. Fig. 7 shows the expected increasing trend of 'Fin Effect' for various technology nodes. Intuitively, one requires tallest fin and smallest fin pitch possible. In FinFET architecture, contact length follows a similar decreasing trend as fin pitch (Fig. 8), which dictates the available contact area per device (see Fig. 9,10) and hence drives an increase in contact resistance (R_C). ρ_C values which represent thermionic, quantum tunneling and fully ohmic regimes are used to calculate R_C for different technology nodes (Fig.11). As contact area decreases, R_C increases and the rate is more pronounced for smaller technology nodes. In order to confirm the correctness of our calculations, three-dimensional TCAD simulations are done for CPP values of 48nm and 37nm using industry scale TCAD tools [7]. It's apparent from Fig.11 that TCAD results are in excellent agreement with existing technologies at 7nm node where CPP=48nm. For short-channel FinFETs device-design-point (DDP) requires $R_{ON}\approx$200-400Ω-µm and $R_C\leq R_{ON}/10$ [1], [8]. Our findings show that for current values of ρ_C at ~2×10^{-9}, R_C is already exceeding the required contact resistance limits for CPP of 48nm. In addition, CPP of 37nm won't be able to satisfy the DDP requirements unless ρ_C values are brought down to quantum tunneling levels. It's not clear to what degree advanced contact structures can help to reduce the contact resistance issues imposed by fin-pitch constrains via geometrical gains in contact area vs. CPP.

Conclusion-In addition to electrostatics challenges, FinFETs scaled below CPP of 40nm will require ρ_C of ~$8\times10^{-10}\Omega$-cm^2 if performance gains are to be extended. Attainment of ρ_C at fully ohmic limit, and/or innovative contact structures, will be required if FinFETs are to extend performance gains below CPP of 30nm, or else a transition to a new device architecture will be required.

References-[1] C. Auth et al., *VLSI Symposium*, p. 131-132, 2012, [2] R. Xie et al., *IEDM Tech. Dig.*, p. 2.7.1, 2016, [3] A. Khakifirooz, *LinkedIn,* 2015, [4] H. Nimi et at., IEEE EDL, pp. 1371-1374, vol. 37 no. 11, 2016, [5] J. Maassen et at., *APL* 102, 111605, 2013, [6] M-H. Na et al., *IEDM Tech. Dig.*, p. 121-124 2002, [7] http://Sentaurus User's Manual, Synopsys, Version K-2015.06, [8] C.-H. Jan et at., *IEDM Tech. Dig.,* p. 28.1.1-28.1.4, 2009, [9] S. Natarajan et al., *IEDM Tech. Dig.*, p.3.7.1, 2014, [10] C.-H. Jan, et al., *IEDM Tech. Dig.*, p 3.1.1, 2012, [11] S.-Y. Wu et al., *IEDM Tech. Dig.*, p. 9.1.1, 2013, [12] K.-I. Seo et al., *VLSI Symposium*, 2014, [13] http://techinsights.com, [14] http://realworldtech.com, [15] http://semiwiki.com, [16] http://chipworks.com, [17] http://semimd.com, [18] http://intel.com, [19] http://archive.eetasia.com, [20] http://electronics-eetimes.com, [21] http://electroiq.com/chipworks_real_chips_blog, [22] *ITRS Roadmap,* 2015 Edition.

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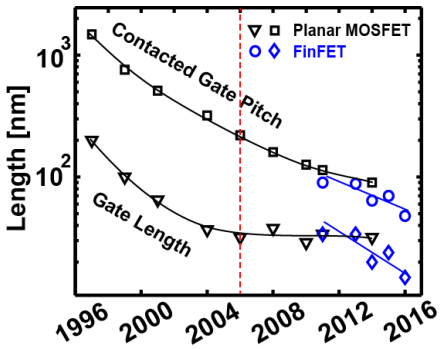

Fig. 1 Introduction of FinFET with more robust electrostatics appeared to be a major breakthrough to resume the gate-length scaling which had reached a plateau at the 65nm node [1-3], [8-21].

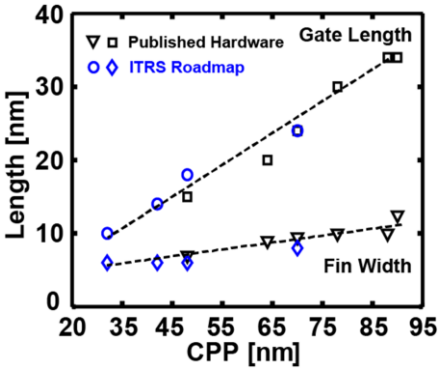

Fig. 2 Gate length and fin width scaling trends vs CPP for various FinFET technologies [1-2], [9-21] and the ITRS Roadmap [22].

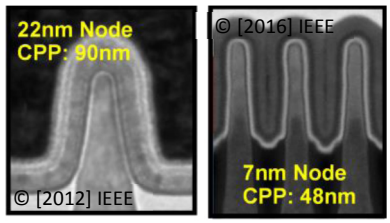

Fig. 3 Cross-sectional TEM images of the Fins for first and last FinFET technologies clearly indicates that Fin profiles have improved towards perfection [1], [2].

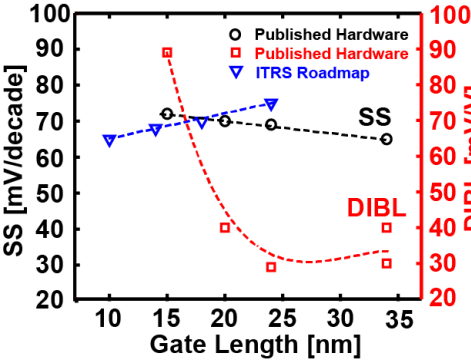

Fig. 4 The opposite trend of subthreshold slope vs CPP compare to ITRS Roadmap is an indication of electrostatic issues in extremely scaled FinFETs. Experimental DIBL data clearly specifies this concern [1-2], [8], [11-12], [22].

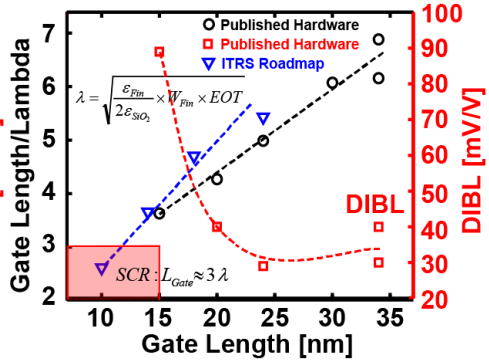

Fig. 5 Ratio of gate to geometrical screening lengths defines the short channel regime for extremely scaled FinFETs, which is supported by the hardware DIBL data [1-2], [8], [11-12], [22].

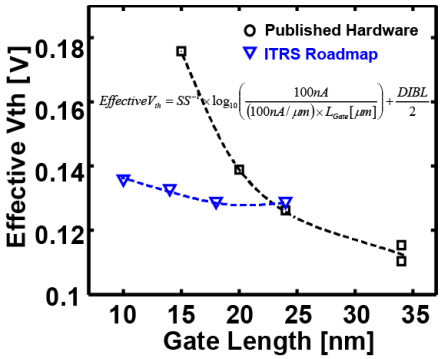

Fig. 6 Calculated effective threshold voltage for existing technologies vs ITRS predictions indicates that FinFET Performance is rapidly deteriorating.

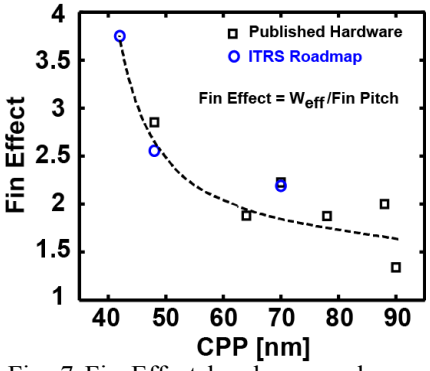

Fig. 7 Fin Effect has been used as a lever to effectively increase the device performance boost.

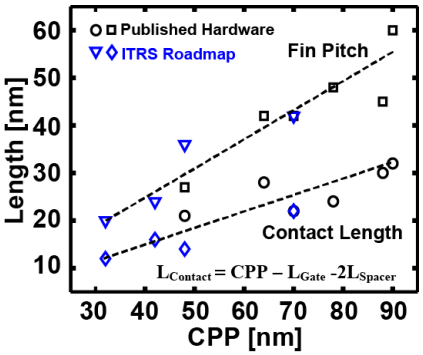

Fig. 8 Calculated contact length scales with a similar trend as fin-pitch for various FinFET technologies.

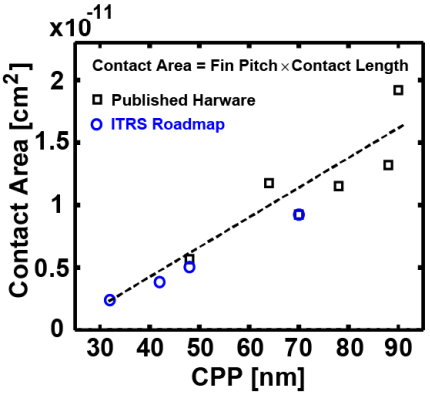

Fig. 9 S/D contact area is rapidly decreasing while FinFETs scale. Area has dropped 75% from the first FinFET technology (22nm node) to the last one (7nm node).

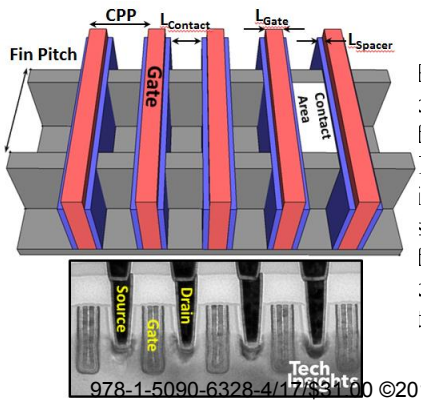

Fig. 10 Critical scaling dimensions are shown for FinFET architecture. TEM cross-sectional image of the same structure parallel to the fin indicates how S/D contacts are landing on the epi.

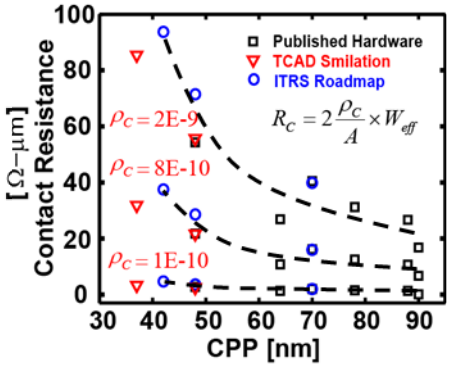

Fig. 11 Contact resistance for thermionic, quantum tunneling and fully ohmic contact resistivity values (ρ_C). R_C will not meet the DDP requirements at CPP <40nm unless contact resistivity is brought down to quantum tunneling levels (~$8\times10^{-10}\Omega$-cm^2).

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