Hitchhiker's Guide
to
VLSI Design Rules in Magic

Trevin Murakami
based on guide by David Money Harris
October 10, 2010

Getting around Linux

The Magic tools run on Red Hat Enterprise Linux Version 5. Basic Linux navigation is essential. Right click on the desktop and open a terminal window to get a command prompt. Common commands are listed below. Most of the commands have options (for example, "`ls -l`" displays a long listing of files in the directory.

`ls`	list files in the directory
	`-l` shows a long listing with permissions, owners, dates, sizes
	`-a` shows all files, even the hidden ones
`cd`	change directory
`pwd`	print working directory
`mkdir`	make a directory
`mv`	move
`cp`	copy
`ln`	make a symbolic link (a.k.a. a shortcut or alias)
`rm`	remove
	`-r`: recursive remove (remove a directory and everything inside it; *dangerous*! ☠)
`top`	display the tasks using the most resources
`more`	display contents of a text file, one screen at a time
`acroread`	view a PDF file using adobe acrobat reader
`man`	display manual pages for a command, where more details are listed

A longer list of commands is at http://www.ss64.com/bash/

Also, make sure you know how to use a text editor, like `emacs`, `vim`, or `nano`.

About the SCN6M Process

The MOSIS 6M process is a 0.9 µm process with 6 metal layers (M1-M6).

The common layers are:

ndiff/pdiff: diffusion
nwell/pwell: wells
poly: polysilicon
pc: contact from Metal1 to polysilicon
ndc/pdc: contact from Metal1 to diffusion
m1 / m2 / m3 / m4 / m5 / m6: Metal 1-6
m2c / m3c / m4c / m5c / m6c: Contacts 2-6 (connects to the metal below)

Simplified Select Design Rules

Structure	Design rule (λ)	Rule #
Poly width (for transistor gates)	2	3.1
Poly spacing	3	3.2
Poly Gate spacing	4 (larger than pc-pc)	3.2.a
NDiff width (minimum transistor width)	3	2.1
PDiff width (minimum transistor width)	3	2.1
Same Diffusion spacing	3	2.2
NDiff to PDiff spacing	12	2.3
Poly overlaps beyond diffusion	3	3.3
Poly spacing to diffusion	1	3.5
PC size	4	5.1
PC to PC spacing	3	7.2
PC to Poly spacing	4	5.5.b
NDC/PDC size	4	5.1
NDC/PDC spacing	3	2.2/7.2
Contact to Diffusion spacing	4	6.5b
NWell width	12	1.1
NWell spacing	6 (same potential)	1.3
NWell spacing from n-diffusion	6	2.3
NWell surround of p-diffusion	6	2.4
NWell surround of n+ well contact	3	2.4
PWell width	12	1.1
PWell spacing	6 (same potential)	1.3
PWell spacing from p-diffusion	6	2.3
PWell surround of n-diffusion	6	2.4
PWell surround of p+ well contact	3	2.4
M1 size	3	7.1
M1 spacing	3	7.2
M2C size	5	8.1
M2C spacing	4	9.2
M2 width	3	9.1
M2 spacing	4	9.2
M3C size	5	14.1
M3C spacing	4	9.2/15.2
M3 width	3	15.1
M3 spacing	4	15.2

When Doing Design...

Make sure you learn the macros. They will speed up your ability to do layout immensely.

Make sure you always do a stick diagram and think about how all your pieces will fit together. Making a slice plan for a long datapath is very important if you want to make it compact.

Example Standardized Cell Rules

These are safe, example rules you can use to help design your layouts.
BE WARNED: many of the rules are intentionally inefficient.
I advise that you use this as a template to design your own rules.

- Start all cells with the lower left corner of Gnd at the origin.
- Cell pitch (ground of one row to ground of the next) is 80λ, bottom of Gnd to bottom of Vdd is 65λ
- Vdd and Gnd run horizontally in 10λ wide Metal1
    - Gnd from 0 to 10
    - Vdd from 65 to 75
- All cells are a multiple of 10λ wide. The multiple is the number of "columns."
- Use only M1 and M2 metal in the cell if possible, M3 if necessary.
- Substrate and well contacts under Vdd and Gnd centered every 10λ
- Input and output ports on Metal2 on a 10λ column pitch
- Control wires run vertically on Metal2 (width = 5λ, spacing = 5λ).
- Bit lines run horizontally on Metal3 (width = 5λ, spacing = 5λ). 7 M3 tracks over each cell.
- Fixed height wells in every cell extending beyond the left and right sides and covering below and above the ground/power rails.
- Maximum nMOS gate width: 12λ (13 to 25)
- Maximum pMOS gate width: 24λ (38 to 62)
- Polysilicon gates should be exactly 2λ wide.
- Generally make M1 and poly wires 5λ wide for easy contacting
- M1 and diffusion should start at least 2λ in from the left border of cell and 3λ from the right border of the cell so that two adjacent cells do not have conflicts.
- Use 5λ x 5λ Metal-to-Metal Contacts

Make sure you check the EEC116 website for more resources.
`ece.ucdavis.edu/~bbaas/116/`